Zynq UltraScale+ MPSoC

ACU11EG System on Module

User Manual

ALINX

Document Revision Record:

Version	Time	Description
1.0	2025/08/06	Initial Release

Table of Contents

1 ACU11EG Core Board

The **ACU11EG** core module is built around the **AMD Xilinx Zynq® UltraScale+™ MPSoC XCZU11EG-2FFVC1156I** device. With compact dimensions of only **80 × 60 mm**, the module provides a powerful yet space-efficient platform ideally suited for secondary development and custom carrier board designs.

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Figure 1-1: ACU11EG Core Board Top View

1.1 Features

- **Memory**
  - 8 × Nanya DDR4 devices (NT5AD512M16C4-JRI), 4 on PS and 4 on PL side
  - 64-bit data bus, **4 GB capacity**, up to **1200 MHz (2400 Mbps)**
  - 2 × 256 Mbit QSPI Flash for boot and configuration storage
  - 1 × 32 GB eMMC Flash for system files
- **Connectivity via four board-to-board connectors**
  - PS side: USB 2.0, Gigabit Ethernet, SD card, and remaining MIO signals
  - 4 × PS MGT transceiver pairs
  - PL side: 16 × MGT transceivers, 134 × HP I/Os, 46 × HD I/Os
- **Design considerations**
  - Length-matched and differential-pair routed signal traces between SoC and connectors
  - Optimized for high-speed and reliable data transmission

1.2 FPGA Chip

1.2.1 ZYNQ Chip

The development board is built with the Xilinx Zynq UltraScale+ MPSoC EG series, specifically the XCZU11EG-2FFVC1156I device.

The overall block diagram of the ZU11EG chip is shown in the figure 1.2.1-1 below.

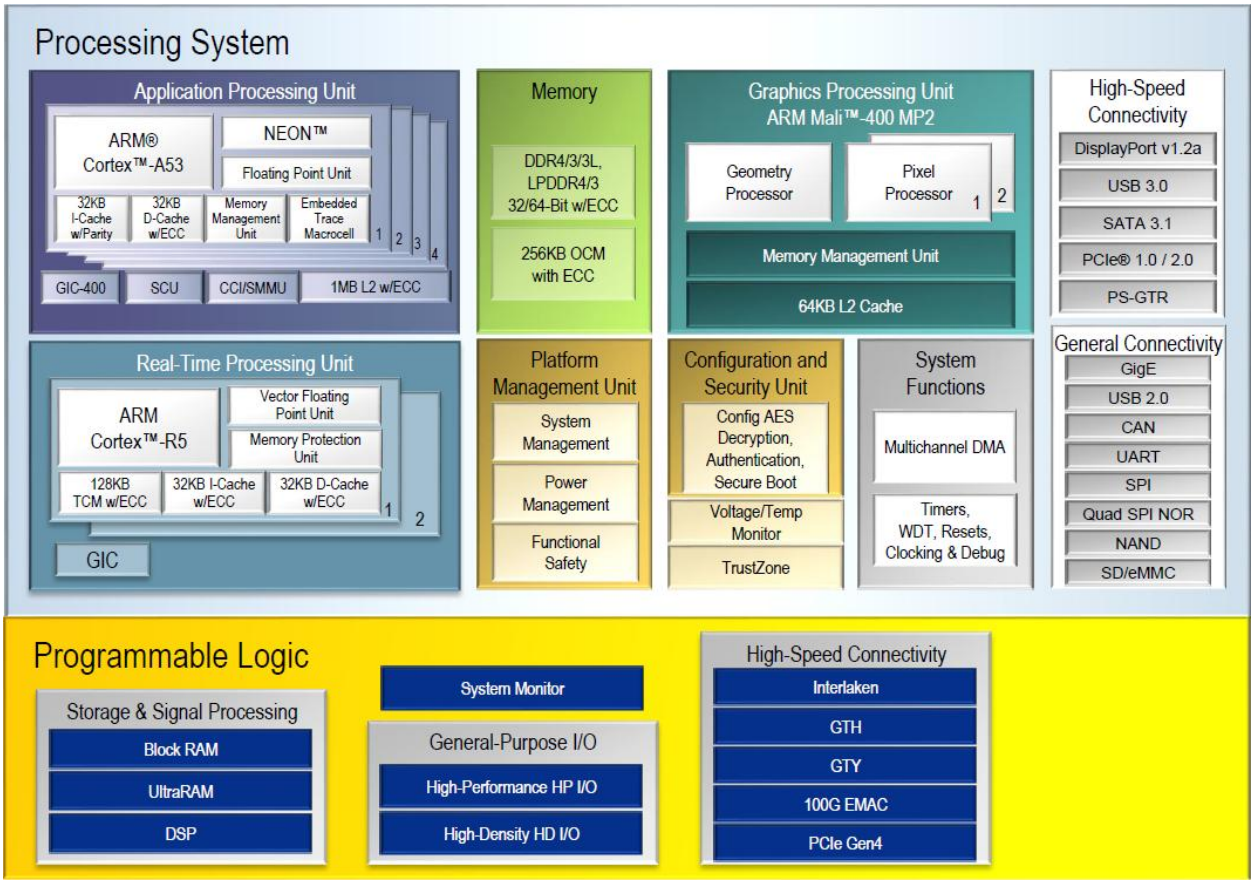


Figure 1.2.1-1: ZYNQ ZU11EG Chip Overview Diagram

Processing System (PS)

- Quad-core ARM Cortex™-A53 processors, up to 1.3GHz, each with 32KB L1 instruction and 32KB L1 data cache, and a shared 1MB L2 cache for every two CPUs.
- Dual-core ARM Cortex-R5 processors, up to 533MHz, each with 32KB L1 instruction and 32KB L1 data cache, plus 128KB Tightly Coupled Memory (TCM).
- Mali-400 MP2 GPU, up to 677MHz, with 64KB L2 cache for graphics and video processing.
- External memory interfaces supporting 32/64-bit DDR4, DDR3/3L, LPDDR4/3.
- Static memory interfaces for NAND Flash and dual Quad-SPI Flash.
- High-speed interfaces: PCIe Gen2 x4, 2 × USB3.0, SATA 3.1, DisplayPort, 4 × Tri-mode Gigabit Ethernet.
- General-purpose interfaces: 2 × USB2.0, 2 × SD/SDIO, 2 × UART, 2 × CAN 2.0B, 2 × I²C, 2 × SPI, 4 × 32-bit GPIO.
- Power management supporting full, low-power, PL-only, and battery power domains.
- Security features: RSA, AES, and SHA hardware acceleration.
- System monitoring: 10-bit, 1Msps ADC for on-chip temperature and voltage monitoring.

Programmable Logic (PL)

- System Logic Cells: 653.1K

- CLB Flip-Flops: 597.12K
- CLB LUTs: 298.56K
- Block RAM: 21.1Mb
- Clock Management Tiles (CMTs): 8
- DSP Slices: 2928
- GTH 16.3Gb/s transceivers: 20

Device Information

- Part Number: XCZU11EG-2FFVC1156I
- Speed Grade: -2
- Package: FFVC1156
- Temperature Grade: Industrial

1.3 DDR4 DRAM

1.3.1 Specifications

DDR4 SDRAM Configuration of ACU11EG Core Board

The ACU11EG core board is equipped with eight NANYA (NT5AD512M16C4-JRI, compatible with MT40A512M16LY-062E) 1GB DDR4 chips.

- PS side: Four DDR4 chips are mounted, forming a 64-bit data bus with a total capacity of 4GB. The maximum operating frequency of the PS-side DDR4 SDRAM is 1200MHz (data rate 2400Mbps). These four DDR4 devices are directly connected to the memory interface of BANK504 in the PS.
- PL side: Four DDR4 chips are mounted, forming a 64-bit data bus with a total capacity of 4GB. The maximum operating frequency of the PL-side DDR4 SDRAM is 1200MHz (data rate 2400Mbps). These four DDR4 devices are connected to the FPGA interfaces of BANK66, BANK67, and BANK68.

The specific configuration of the PS and PL DDR4 SDRAM is shown in Table 1.3.1-1.

Location	Designator	Chip Model	Capacity	Manufacture
PS	U4,U5,U6,U7	NT5AD512M16C4-JRI	512M x 16bit	Nanya
PL	U17,U19,U45,U46	NT5AD512M16C4-JRI	512M x 16bit	Nanya

Table 1.3.1-1: DDR4 SDRAM Configuration

In DDR4 hardware design, strict consideration must be given to signal integrity. In our circuit and PCB design, we have fully considered matching resistors/termination resistors, trace impedance control, and length matching, ensuring stable high-speed operation of DDR4.

The hardware connection of the PS-side DDR4 is illustrated in Figure1.3.1-1 below:

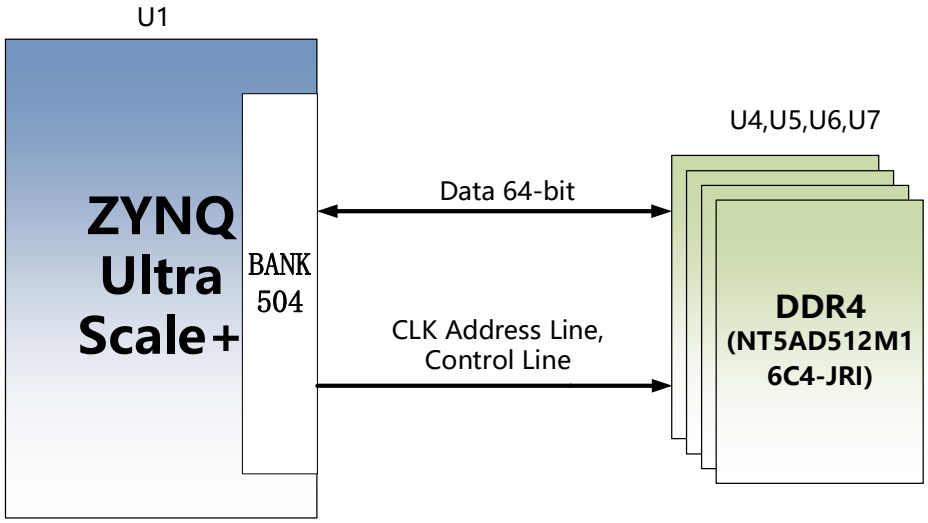


Figure 1.3.1-1: PS-side DDR4 DRAM Schematic

The hardware connection of the PL-side DDR4 is illustrated in Figure 1.3.1-2 below:

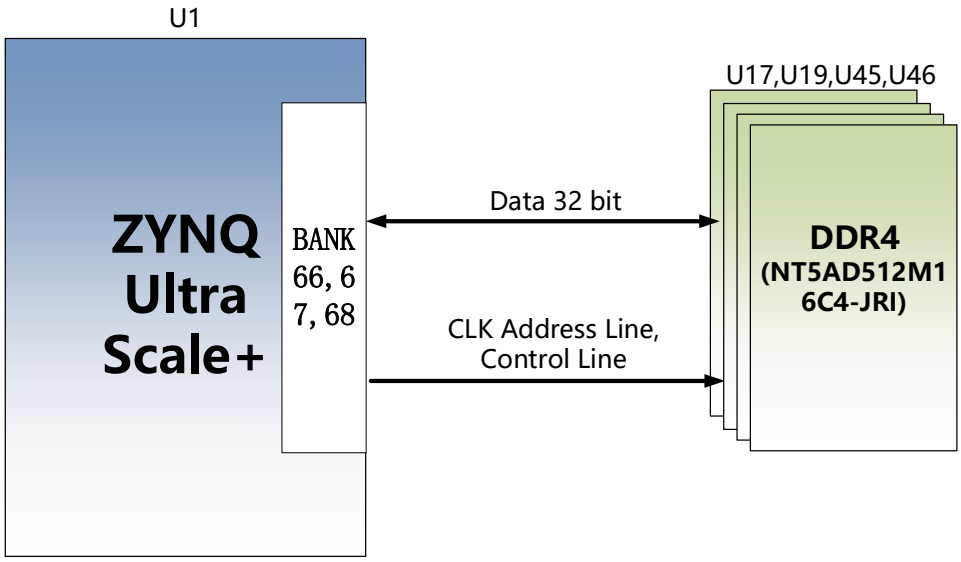


Figure 1.3.1-2: PL-side DDR4 DRAM Schematic

1.3.2 PS Side DDR4 SDRAM Pin Assignment

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	AN27
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AN26
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AP30
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AN29
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AJ26
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AH26
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AK29
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AK28
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AD31
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AD30
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	Y28
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	Y27
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AB34
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AB33
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	W32
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	W31
PS_DDR4_DQ0	PS_DDR_DQ0_504	AP27
PS_DDR4_DQ1	PS_DDR_DQ1_504	AP25
PS_DDR4_DQ2	PS_DDR_DQ2_504	AP26
PS_DDR4_DQ3	PS_DDR_DQ3_504	AM26
PS_DDR4_DQ4	PS_DDR_DQ4_504	AP24
PS_DDR4_DQ5	PS_DDR_DQ5_504	AL25
PS_DDR4_DQ6	PS_DDR_DQ6_504	AM25
PS_DDR4_DQ7	PS_DDR_DQ7_504	AM24
PS_DDR4_DQ8	PS_DDR_DQ8_504	AM28

PS_DDR4_DQ9	PS_DDR_DQ9_504	AN28
PS_DDR4_DQ10	PS_DDR_DQ10_504	AP29
PS_DDR4_DQ11	PS_DDR_DQ11_504	AP28
PS_DDR4_DQ12	PS_DDR_DQ12_504	AM31
PS_DDR4_DQ13	PS_DDR_DQ13_504	AP31
PS_DDR4_DQ14	PS_DDR_DQ14_504	AN31
PS_DDR4_DQ15	PS_DDR_DQ15_504	AM30
PS_DDR4_DQ16	PS_DDR_DQ16_504	AF25
PS_DDR4_DQ17	PS_DDR_DQ17_504	AG25
PS_DDR4_DQ18	PS_DDR_DQ18_504	AG26
PS_DDR4_DQ19	PS_DDR_DQ19_504	AJ25
PS_DDR4_DQ20	PS_DDR_DQ20_504	AG24
PS_DDR4_DQ21	PS_DDR_DQ21_504	AK25
PS_DDR4_DQ22	PS_DDR_DQ22_504	AJ24
PS_DDR4_DQ23	PS_DDR_DQ23_504	AK24
PS_DDR4_DQ24	PS_DDR_DQ24_504	AH28
PS_DDR4_DQ25	PS_DDR_DQ25_504	AH27
PS_DDR4_DQ26	PS_DDR_DQ26_504	AJ27
PS_DDR4_DQ27	PS_DDR_DQ27_504	AK27
PS_DDR4_DQ28	PS_DDR_DQ28_504	AL26
PS_DDR4_DQ29	PS_DDR_DQ29_504	AL27
PS_DDR4_DQ30	PS_DDR_DQ30_504	AH29
PS_DDR4_DQ31	PS_DDR_DQ31_504	AL28
PS_DDR4_DQ32	PS_DDR_DQ32_504	AB29
PS_DDR4_DQ33	PS_DDR_DQ33_504	AB30
PS_DDR4_DQ34	PS_DDR_DQ34_504	AC29
PS_DDR4_DQ35	PS_DDR_DQ35_504	AD32
PS_DDR4_DQ36	PS_DDR_DQ36_504	AC31
PS_DDR4_DQ37	PS_DDR_DQ37_504	AE30
PS_DDR4_DQ38	PS_DDR_DQ38_504	AC28
PS_DDR4_DQ39	PS_DDR_DQ39_504	AE29
PS_DDR4_DQ40	PS_DDR_DQ40_504	AC27
PS_DDR4_DQ41	PS_DDR_DQ41_504	AA27
PS_DDR4_DQ42	PS_DDR_DQ42_504	AA28
PS_DDR4_DQ43	PS_DDR_DQ43_504	AB28
PS_DDR4_DQ44	PS_DDR_DQ44_504	W27
PS_DDR4_DQ45	PS_DDR_DQ45_504	W29
PS_DDR4_DQ46	PS_DDR_DQ46_504	W28
PS_DDR4_DQ47	PS_DDR_DQ47_504	V27
PS_DDR4_DQ48	PS_DDR_DQ48_504	AA32
PS_DDR4_DQ49	PS_DDR_DQ49_504	AA33
PS_DDR4_DQ50	PS_DDR_DQ50_504	AA34
PS_DDR4_DQ51	PS_DDR_DQ51_504	AE34

PS_DDR4_DQ52	PS_DDR_DQ52_504	AD34
PS_DDR4_DQ53	PS_DDR_DQ53_504	AB31
PS_DDR4_DQ54	PS_DDR_DQ54_504	AC34
PS_DDR4_DQ55	PS_DDR_DQ55_504	AC33
PS_DDR4_DQ56	PS_DDR_DQ56_504	AA30
PS_DDR4_DQ57	PS_DDR_DQ57_504	Y30
PS_DDR4_DQ58	PS_DDR_DQ58_504	AA31
PS_DDR4_DQ59	PS_DDR_DQ59_504	W30
PS_DDR4_DQ60	PS_DDR_DQ60_504	Y33
PS_DDR4_DQ61	PS_DDR_DQ61_504	W33
PS_DDR4_DQ62	PS_DDR_DQ62_504	W34
PS_DDR4_DQ63	PS_DDR_DQ63_504	Y34
PS_DDR4_DM0	PS_DDR_DM0_504	AN24
PS_DDR4_DM1	PS_DDR_DM1_504	AM29
PS_DDR4_DM2	PS_DDR_DM2_504	AH24
PS_DDR4_DM3	PS_DDR_DM3_504	AJ29
PS_DDR4_DM4	PS_DDR_DM4_504	AD29
PS_DDR4_DM5	PS_DDR_DM5_504	Y29
PS_DDR4_DM6	PS_DDR_DM6_504	AC32
PS_DDR4_DM7	PS_DDR_DM7_504	Y32
PS_DDR4_A0	PS_DDR_A0_504	AN34
PS_DDR4_A1	PS_DDR_A1_504	AM34
PS_DDR4_A2	PS_DDR_A2_504	AM33
PS_DDR4_A3	PS_DDR_A3_504	AL34
PS_DDR4_A4	PS_DDR_A4_504	AL33
PS_DDR4_A5	PS_DDR_A5_504	AK33
PS_DDR4_A6	PS_DDR_A6_504	AK30
PS_DDR4_A7	PS_DDR_A7_504	AJ30
PS_DDR4_A8	PS_DDR_A8_504	AJ31
PS_DDR4_A9	PS_DDR_A9_504	AH31
PS_DDR4_A10	PS_DDR_A10_504	AG31
PS_DDR4_A11	PS_DDR_A11_504	AF31
PS_DDR4_A12	PS_DDR_A12_504	AG30
PS_DDR4_A13	PS_DDR_A13_504	AF30
PS_DDR4_ODT0	PS_DDR_ODT0_504	AP32
PS_DDR4_PARITY	PS_DDR_PARITY_504	AA26
PS_DDR4_RAS_B	PS_DDR_A16_504	AF28
PS_DDR4_RESET_B	PS_DDR_RAM_RST_N_504	AD26
PS_DDR4_WE_B	PS_DDR_A14_504	AG29
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AE25
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AB26
PS_DDR4_BA0	PS_DDR_BA0_504	AE27
PS_DDR4_BA1	PS_DDR_BA1_504	AE28

PS_DDR4_BG0	PS_DDR_BG0_504	AD27
PS_DDR4_CAS_B	PS_DDR_A15_504	AG28
PS_DDR4_CKE0	PS_DDR_CKE0_504	AN33
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AP33
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	AN32
PS_DDR4_CLK0_P	PS_DDR_CK0_504	AL31

1.3.3 PL Side DDR4 SDRAM Pin Assignment

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_N	IO_L22N_T3U_N7_DBC_AD0N_67	B19
PL_DDR4_DQS0_P	IO_L22P_T3U_N6_DBC_AD0P_67	B18
PL_DDR4_DQS1_N	IO_L10N_T1U_N7_QBC_AD4N_67	F20
PL_DDR4_DQS1_P	IO_L10P_T1U_N6_QBC_AD4P_67	G20
PL_DDR4_DQS2_N	IO_L4N_T0U_N7_DBC_AD7N_67	K23
PL_DDR4_DQS2_P	IO_L4P_T0U_N6_DBC_AD7P_67	K22
PL_DDR4_DQS3_N	IO_L16N_T2U_N7_QBC_AD3N_67	D24
PL_DDR4_DQS3_P	IO_L16P_T2U_N6_QBC_AD3P_67	E24
PL_DDR4_DQS4_N	IO_L4N_T0U_N7_DBC_AD7N_68	B13
PL_DDR4_DQS4_P	IO_L4P_T0U_N6_DBC_AD7P_68	B14
PL_DDR4_DQS5_N	IO_L10N_T1U_N7_QBC_AD4N_68	F13
PL_DDR4_DQS5_P	IO_L10P_T1U_N6_QBC_AD4P_68	G14
PL_DDR4_DQS6_N	IO_L22N_T3U_N7_DBC_AD0N_68	K15
PL_DDR4_DQS6_P	IO_L22P_T3U_N6_DBC_AD0P_68	L15
PL_DDR4_DQS7_N	IO_L16N_T2U_N7_QBC_AD3N_68	H17
PL_DDR4_DQS7_P	IO_L16P_T2U_N6_QBC_AD3P_68	H18
PL_DDR4_DQ0	IO_L21N_T3L_N5_AD8N_67	A21
PL_DDR4_DQ1	IO_L24N_T3U_N11_67	B21
PL_DDR4_DQ2	IO_L23N_T3U_N9_67	A23
PL_DDR4_DQ3	IO_L24P_T3U_N10_67	B20
PL_DDR4_DQ4	IO_L21P_T3L_N4_AD8P_67	A20
PL_DDR4_DQ5	IO_L20N_T3L_N3_AD1N_67	C19
PL_DDR4_DQ6	IO_L23P_T3U_N8_67	A22
PL_DDR4_DQ7	IO_L20P_T3L_N2_AD1P_67	C18
PL_DDR4_DQ8	IO_L12N_T1U_N11_GC_67	F21
PL_DDR4_DQ9	IO_L12P_T1U_N10_GC_67	G21
PL_DDR4_DQ10	IO_L11N_T1U_N9_GC_67	E22
PL_DDR4_DQ11	IO_L9P_T1L_N4_AD12P_67	D20
PL_DDR4_DQ12	IO_L8N_T1L_N3_AD5N_67	H22
PL_DDR4_DQ13	IO_L8P_T1L_N2_AD5P_67	H21
PL_DDR4_DQ14	IO_L11P_T1U_N8_GC_67	F22
PL_DDR4_DQ15	IO_L9N_T1L_N5_AD12N_67	D21
PL_DDR4_DQ16	IO_L2N_T0L_N3_67	K24
PL_DDR4_DQ17	IO_L3N_T0L_N5_AD15N_67	J22

PL_DDR4_DQ18	IO_L6P_T0U_N10_AD6P_67	J24
PL_DDR4_DQ19	IO_L6N_T0U_N11_AD6N_67	H24
PL_DDR4_DQ20	IO_L5P_T0U_N8_AD14P_67	J25
PL_DDR4_DQ21	IO_L2P_T0L_N2_67	L23
PL_DDR4_DQ22	IO_L5N_T0U_N9_AD14N_67	H26
PL_DDR4_DQ23	IO_L3P_T0L_N4_AD15P_67	J21
PL_DDR4_DQ24	IO_L14P_T2L_N2_GC_67	G23
PL_DDR4_DQ25	IO_L15N_T2L_N5_AD11N_67	C22
PL_DDR4_DQ26	IO_L18P_T2U_N10_AD2P_67	G25
PL_DDR4_DQ27	IO_L17P_T2U_N8_AD10P_67	D22
PL_DDR4_DQ28	IO_L14N_T2L_N3_GC_67	G24
PL_DDR4_DQ29	IO_L15P_T2L_N4_AD11P_67	C21
PL_DDR4_DQ30	IO_L18N_T2U_N11_AD2N_67	G26
PL_DDR4_DQ31	IO_L17N_T2U_N9_AD10N_67	C23
PL_DDR4_DQ32	IO_L3P_T0L_N4_AD15P_68	A15
PL_DDR4_DQ33	IO_L6P_T0U_N10_AD6P_68	C13
PL_DDR4_DQ34	IO_L3N_T0L_N5_AD15N_68	A14
PL_DDR4_DQ35	IO_L5N_T0U_N9_AD14N_68	A12
PL_DDR4_DQ36	IO_L2N_T0L_N3_68	B15
PL_DDR4_DQ37	IO_L6N_T0U_N11_AD6N_68	C12
PL_DDR4_DQ38	IO_L2P_T0L_N2_68	B16
PL_DDR4_DQ39	IO_L5P_T0U_N8_AD14P_68	A13
PL_DDR4_DQ40	IO_L9N_T1L_N5_AD12N_68	E17
PL_DDR4_DQ41	IO_L12N_T1U_N11_GC_68	E14
PL_DDR4_DQ42	IO_L9P_T1L_N4_AD12P_68	E18
PL_DDR4_DQ43	IO_L11N_T1U_N9_GC_68	D14
PL_DDR4_DQ44	IO_L8N_T1L_N3_AD5N_68	C17
PL_DDR4_DQ45	IO_L12P_T1U_N10_GC_68	E15
PL_DDR4_DQ46	IO_L8P_T1L_N2_AD5P_68	D17
PL_DDR4_DQ47	IO_L11P_T1U_N8_GC_68	D15
PL_DDR4_DQ48	IO_L21P_T3L_N4_AD8P_68	K17
PL_DDR4_DQ49	IO_L24P_T3U_N10_68	L17
PL_DDR4_DQ50	IO_L20N_T3L_N3_AD1N_68	J15
PL_DDR4_DQ51	IO_L24N_T3U_N11_68	L16
PL_DDR4_DQ52	IO_L21N_T3L_N5_AD8N_68	J17
PL_DDR4_DQ53	IO_L23P_T3U_N8_68	K19
PL_DDR4_DQ54	IO_L20P_T3L_N2_AD1P_68	J16
PL_DDR4_DQ55	IO_L23N_T3U_N9_68	K18
PL_DDR4_DQ56	IO_L17P_T2U_N8_AD10P_68	G18
PL_DDR4_DQ57	IO_L18P_T2U_N10_AD2P_68	H16
PL_DDR4_DQ58	IO_L17N_T2U_N9_AD10N_68	F18
PL_DDR4_DQ59	IO_L14P_T2L_N2_GC_68	G15
PL_DDR4_DQ60	IO_L15N_T2L_N5_AD11N_68	G19

PL_DDR4_DQ61	IO_L15P_T2L_N4_AD11P_68	H19
PL_DDR4_DQ62	IO_L14N_T2L_N3_GC_68	F15
PL_DDR4_DQ63	IO_L18N_T2U_N11_AD2N_68	G16
PL_DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_67	A18
PL_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_67	E19
PL_DDR4_DM2	IO_L1P_T0L_N0_DBC_67	L21
PL_DDR4_DM3	IO_L13P_T2L_N0_GC_QBC_67	F23
PL_DDR4_DM4	IO_L1P_T0L_N0_DBC_68	A17
PL_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_68	D16
PL_DDR4_DM6	IO_L19P_T3L_N0_DBC_AD9P_68	L20
PL_DDR4_DM7	IO_L13P_T2L_N0_GC_QBC_68	F17
PL_DDR4_A0	IO_L10P_T1U_N6_QBC_AD4P_66	AK8
PL_DDR4_A1	IO_L6P_T0U_N10_AD6P_66	AM9
PL_DDR4_A2	IO_L10N_T1U_N7_QBC_AD4N_66	AL8
PL_DDR4_A3	IO_L5N_T0U_N9_AD14N_66	AM10
PL_DDR4_A4	IO_L11N_T1U_N9_GC_66	AK10
PL_DDR4_A5	IO_L3N_T0L_N5_AD15N_66	AP11
PL_DDR4_A6	IO_L14N_T2L_N3_GC_66	AJ11
PL_DDR4_A7	IO_L4P_T0U_N6_DBC_AD7P_66	AN9
PL_DDR4_A8	IO_L17N_T2U_N9_AD10N_66	AG10
PL_DDR4_A9	IO_L6N_T0U_N11_AD6N_66	AM8
PL_DDR4_A10	IO_L11P_T1U_N8_GC_66	AJ10
PL_DDR4_A11	IO_L5P_T0U_N8_AD14P_66	AM11
PL_DDR4_A12	IO_L9N_T1L_N5_AD12N_66	AL12
PL_DDR4_A13	IO_L4N_T0U_N7_DBC_AD7N_66	AN8
PL_DDR4_ODT	IO_L16P_T2U_N6_QBC_AD3P_66	AG9
PL_DDR4_BA1	IO_L3P_T0L_N4_AD15P_66	AN11
PL_DDR4_BA0	IO_L7N_T1L_N1_QBC_AD13N_66	AL13
PL_DDR4_BG0	IO_L7P_T1L_N0_QBC_AD13P_66	AK13
PL_DDR4_CAS_B	IO_L8N_T1L_N3_AD5N_66	AL10
PL_DDR4_RAS_B	IO_L8P_T1L_N2_AD5P_66	AL11
PL_DDR4_CS_B	IO_L9P_T1L_N4_AD12P_66	AK12
PL_DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_66	AJ12
PL_DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_66	AH12
PL_DDR4_WE_B	IO_L15N_T2L_N5_AD11N_66	AH13
PL_DDR4_CKE	IO_L15P_T2L_N4_AD11P_66	AG13
PL_DDR4_ACT_B	IO_L16N_T2U_N7_QBC_AD3N_66	AH9
PL_DDR4_RST	IO_L14P_T2L_N2_GC_66	AH11

1.4 QSPI Flash

1.4.1 Schematics

The ACU11EG core board is equipped with two 256 Mbit Quad-SPI FLASH chips, model number MT25QU256ABA1EW9, which are configured to form an 8-bit data bus. These chips use a 1.8V CMOS voltage standard.

Due to its non-volatile nature, the QSPI FLASH can be used as a boot device to store the system's boot images. These images can include the FPGA bitstream, ARM application code, and other user data files.

The specific model and related parameters of the QSPI FLASH are shown in Table 1.4.1-1.

Designator	Chip Model	Capacity	Manufacture
U2,U3	MT25QU256ABA1EW9	256M bit	Micron

Table 1.4.1-1: QSPI Flash Model & Specification

The QSPI FLASH is connected to the GPIO pins of the Zynq chip's PS (Processing System) section in BANK500. In the system design, these PS-side pins must be configured to function as the QSPI FLASH interface. Figure 2.5 shows the relevant section of the QSPI Flash schematic.

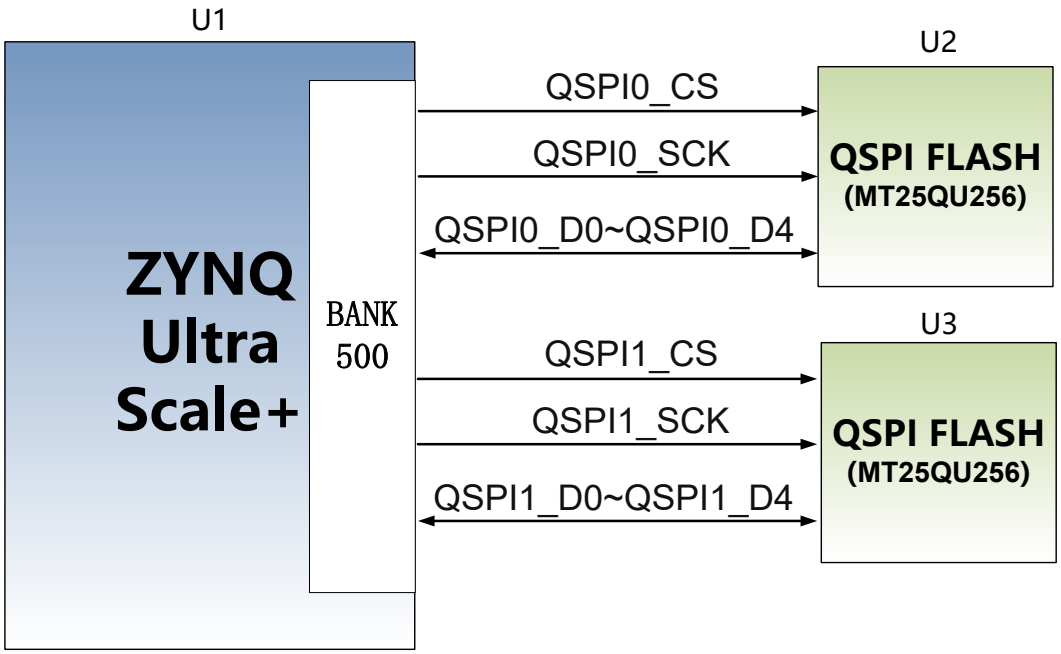


Figure 1.4.1-1: QSPI Flash Connection Diagram

1.4.2 Configuration Device Pin Assignment:

Signal Name	Pin Name	Pin Number
MIO0_QSPI0_SCLK	PS_MIO0_500	A24
MIO1_QSPI0_IO1	PS_MIO1_500	C24
MIO2_QSPI0_IO2	PS_MIO2_500	B24
MIO3_QSPI0_IO3	PS_MIO3_500	E25
MIO4_QSPI0_IO0	PS_MIO4_500	A25
MIO5_QSPI0_SS_B	PS_MIO5_500	D25
MIO10_QSPI1_IO2	PS_MIO10_500	F26
MIO11_QSPI1_IO3	PS_MIO11_500	B26

MIO12_QSPI1_SCLK	PS_MIO12_500	C27
MIO7_QSPI1_SS_B	PS_MIO7_500	B25
MIO8_QSPI1_IO0	PS_MIO8_500	D26
MIO9_QSPI1_IO1	PS_MIO9_500	C26

1.5 eMMC Flash

1.5.1 Schematics

The ACU11EG core board is equipped with a high-capacity 32GB eMMC FLASH chip, model number MTFC32GAPALBH-IT. It supports the JEDEC e-MMC V5.0 standard HS-MMC interface and is compatible with both 1.8V and 3.3V I/O levels. The data width of the connection between the eMMC FLASH and the Zynq is 8-bit.

Due to its high capacity and non-volatile nature, the eMMC FLASH serves as a large-scale storage device in the Zynq system. It can be used for storing ARM applications, system files, and other user data.

The specific model and related parameters of the eMMC FLASH are shown in Table 1.5.1-1.

Reference Designator	Chip Model	Capacity	Manufacture
U8	MTFC32GAKAJCN-4M	32G Byte	Micron

Table 1.5.1-1*: eMMC Flash Model & Specification*

The eMMC FLASH is connected to the GPIO pins of the Zynq UltraScale+ **PS** (Processing System) section in **BANK500**. In the system design, these PS-side GPIO pins must be configured to function as the eMMC interface. Figure 1.5.1-1 shows the relevant section of the eMMC Flash schematic.

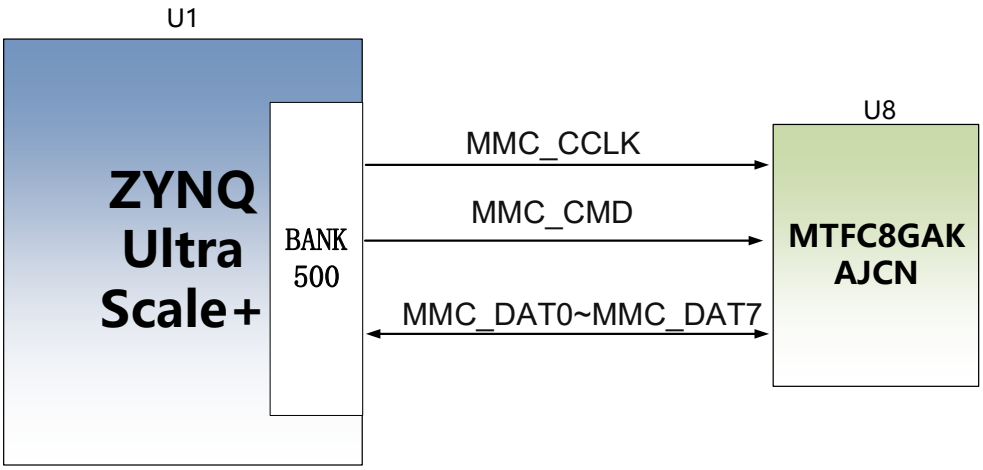


Figure 1.5.1-1: eMMC Flash Connection Diagram

1.5.2 Chip Pin Assignment

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	F28
MMC_CMD	PS_MIO21_500	C28
MMC_DAT0	PS_MIO13_500	D27
MMC_DAT1	PS_MIO14_500	A27
MMC_DAT2	PS_MIO15_500	E27

MMC_DAT3	PS_MIO16_500	A28
MMC_DAT4	PS_MIO17_500	C29
MMC_DAT5	PS_MIO18_500	F27
MMC_DAT6	PS_MIO19_500	B28
MMC_DAT7	PS_MIO20_500	E29
MMC_RSTN	PS_MIO23_500	B29

Table 1.5.2: Chip Pin Assignment

1.6 CLK Configuration

1.6.1 200MHz Differential Clock Source

The core board provides independent reference clocks for the PS and the PL sections, as well as an RTC (Real-Time Clock). This allows the PS and PL to operate independently. A schematic of the clock circuit design is shown in Figure 1.6.1-1below.

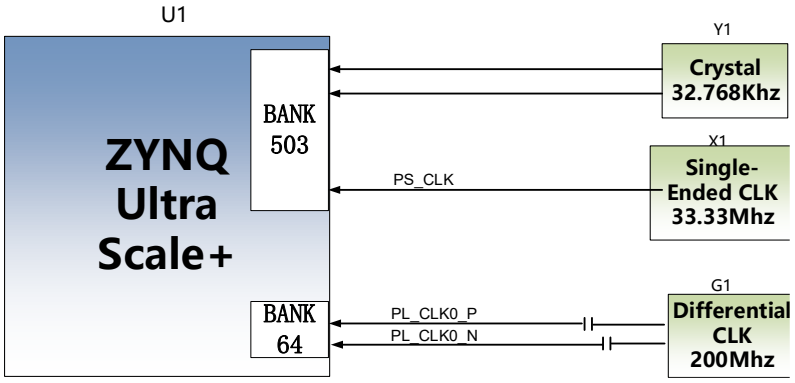


Figure 1.6.1-1: Clock Source Schematics

1.6.2 PS System Real Time Clock(RTC)

The Y1 crystal resonator on the core board provides a 32.768KHz source for the PS system's Real-Time Clock. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of the Zynq chip's BANK503. Its schematic is shown in Figure 1.6.2-1.

Figure 1.6.2-1: RTC Crystal Resonator

1.6.3 CLK Pin Assignment:

Signal Name	PIN
PS_PADI_503	**M25**
PS_PADO_503	**L25**

1.6.4 PS System Clock Source

The X1 oscillator on the core board provides a 33.333MHz clock input for the PS section. The clock input is connected to the PS_REF_CLK_503 pin of the Zynq chip's BANK503. Its schematic is shown in Figure 1.6.4-1.

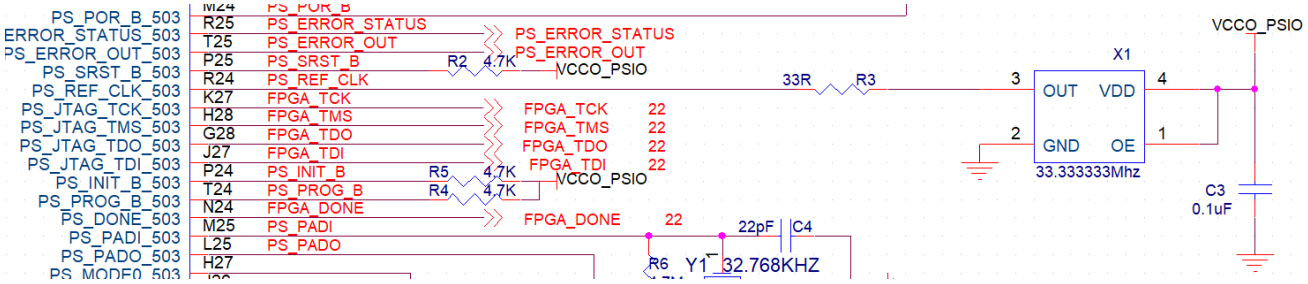


Figure 1.6.4-1: PS Side CLK source

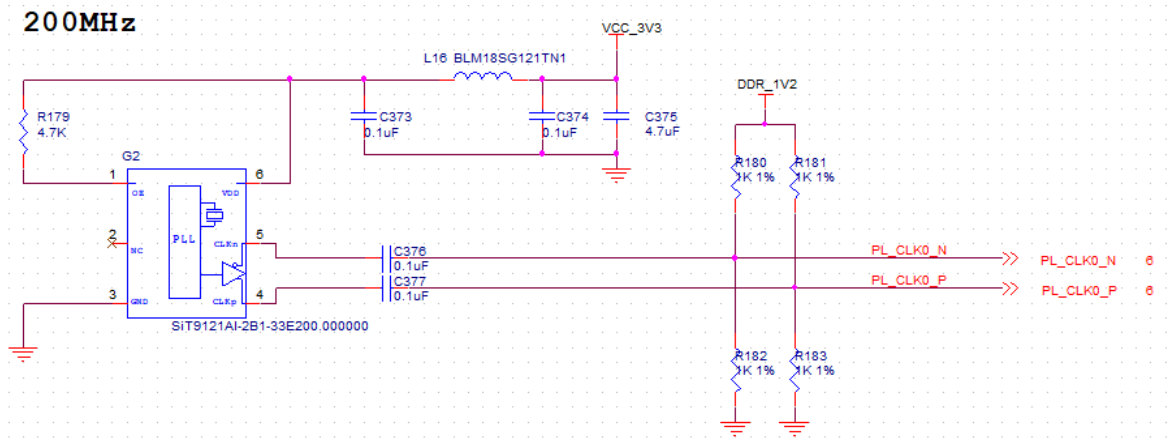
PS CLK PIN Assignment:

Signal Name	PIN
PS_REF_CLK	R24

Figure 1.6.4-1: PS Section Active Oscillator

1.6.5 PL System Clock Source

A 200MHz differential PL system clock source is provided on the board to serve as a reference clock for the DDR4 controller. The oscillator's output is connected to a global clock input (MRCC) of PL BANK64. This global clock can be used to drive the DDR4 controller and other user logic circuits within the FPGA. The schematic for this clock source is shown in Figure 1.6.5-1



1.6.6 PL CLK PIN Assignment:

Signal Name	PIN
PL_CLK0_P	AJ9
PL_CLK0_N	AK9

1.7 Power Supply

ACU11EG core board is powered by a +12V supply, provided through a connection to a carrier board. On the core board, two MYMGM1R824ELA5RP power chips are used in parallel to provide the 0.85V core voltage for the XCZU11EG, supplying up to 50A of current. The power supplies for BANK28, BANK64, and BANK65 are generated by LDOs, with a default voltage of 1.8V. Users can replace these LDOs to change the I/O voltage standard, but it should be noted that the supply voltage for these banks must not exceed 1.8V.

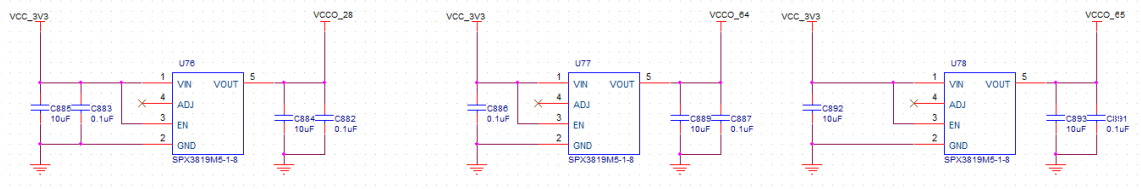


Figure 1.7-1: QSPI Flash type and parameter.

Additionally, a TPS6508640 PMIC (Power Management IC) is used on the board to generate all other required power supplies for the XCZU11EG chip. For the TPS6508640 power design, please refer to the power chip's datasheet. A block diagram of the design is shown below.

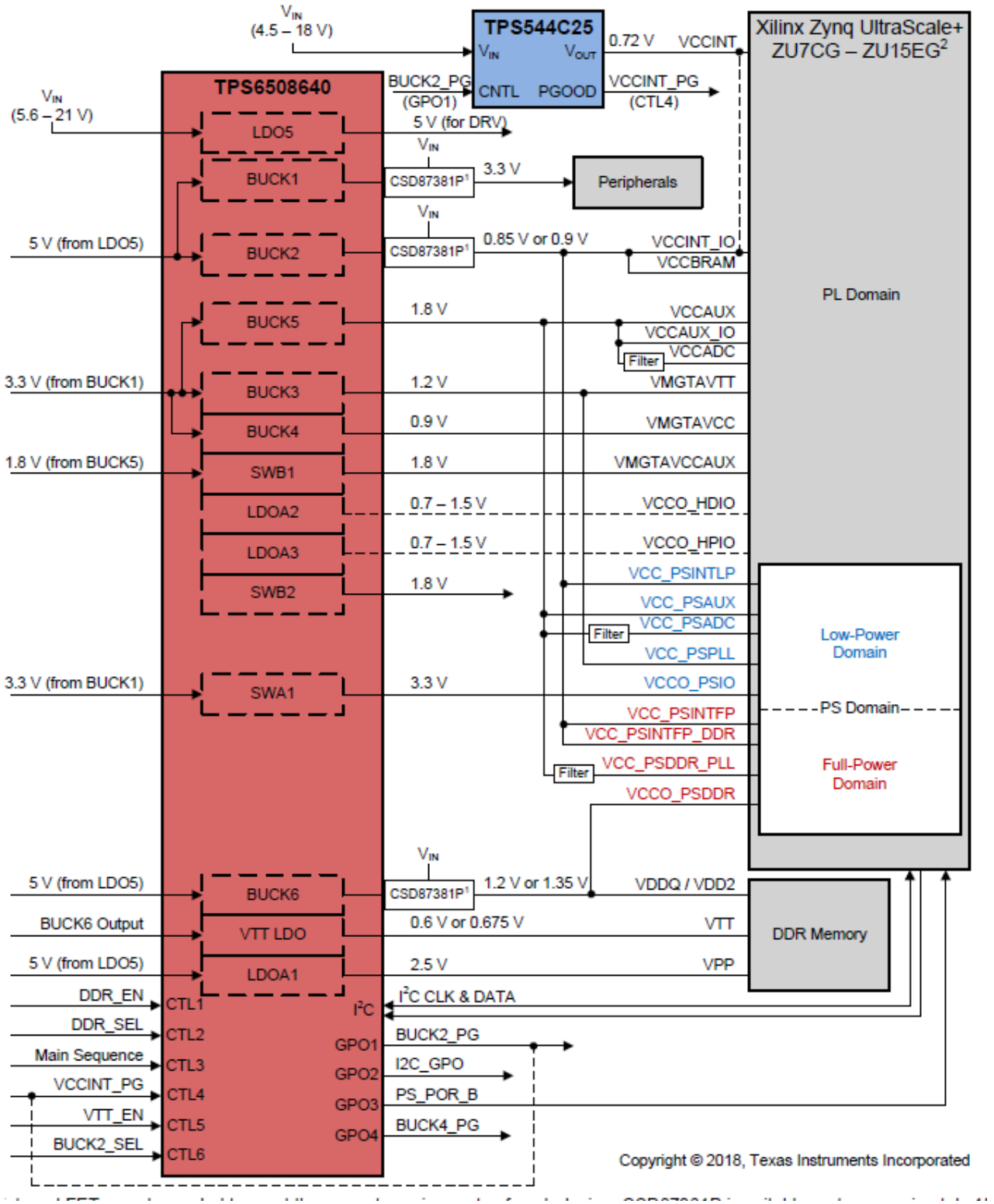


Figure 1.7-2: QSPI Flash type and parameter

1.8 Schematic

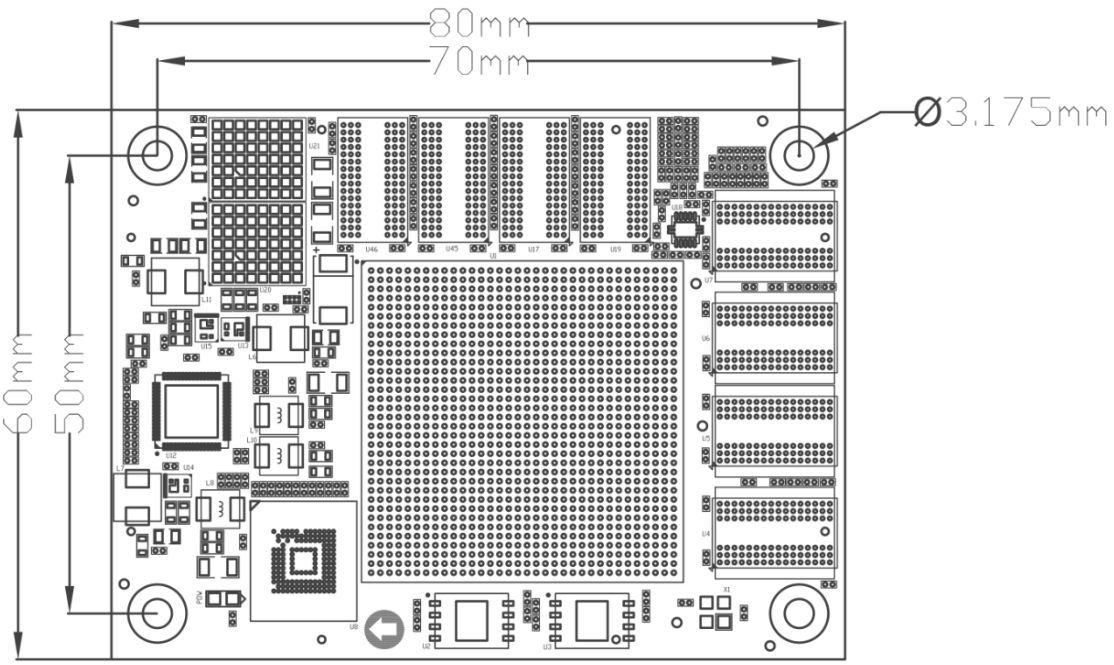


Figure 1.8-1: Top View

1.9Connector Pin Definitions

The core board provides a total of four high-speed expansion connectors, using four 120-pin board-to-board connectors (J29-J32) to interface with a carrier board. The connectors used on the core board are Panasonic AXK5A2137YG, which mate with AXK6A2337YG on the carrier board

J29 Connector

The J29 connector carries the +12V power supply, I/O for BANK69, BANK88, BANK89, and some MIO pins. The I/O voltage standard is 3.3V for BANK88 and BANK89, while the standard for BANK69 and the PS MIO pins is 1.8V.

J29 Pin	Signal name	Pin Number	J29 Pin	Signal name	Pin Number
1	+12V		2	+12V	
3	+12V		4	+12V	
5	+12V		6	+12V	
7	+12V		8	+12V	
9	+12V		10	+12V	
11	+12V		12	+12V	
13	GND		14	GND	
15	B89_L2_N	B1	16	B89_L1_N	D1
17	B89_L2_P	C1	18	B89_L1_P	E1
19	GND		20	GND	
21	B89_L5_N	C2	22	B89_L4_N	E2
23	B89_L5_P	D2	24	B89_L4_P	E3
25	B89_L8_N	D4	26	B89_L3_N	A2
27	B89_L8_P	E4	28	B89_L3_P	A3
29	GND		30	GND	
31	B89_L7_N	B4	32	B89_L6_N	B3
33	B89_L7_P	C4	34	B89_L6_P	C3
35	B89_L9_N	F4	36	B89_L10_N	A5
37	B89_L9_P	F5	38	B89_L10_P	B5
39	GND		40	GND	
41	B89_L11_N	D5	42	B89_L12_N	E5
43	B89_L11_P	D6	44	B89_L12_P	F6
45	B88_L9_N	J6	46	B88_L10_N	G6
47	B88_L9_P	J7	48	B88_L10_P	H6
49	GND	N1	50	GND	
51	B88_L11_N	G7	52	B88_L3_N	M12
53	B88_L11_P	H7	54	B88_L3_P	N13
55	B88_L5_N	M8	56	B88_L12_N	G8
57	B88_L5_P	M9	58	B88_L12_P	H8
59	GND		60	GND	
61	B88_L8_N	J9	62	B88_L7_N	K8
63	B88_L8_P	K9	64	B88_L7_P	L8
65	B88_L2_N	N8	66	B88_L6_N	L10
67	B88_L2_P	N9	68	B88_L6_P	M10
69	GND		70	GND	
71	B88_L4_N	M11	72	B69_L7_N	E7
73	B88_L4_P	N11	74	B69_L7_P	F7
75	B69_L20_N	B8	76	B69_L21_N	A6
77	B69_L20_P	B9	78	B69_L21_P	B6
79	GND		80	GND	
81	B69_L8_N	C8	82	B69_L23_N	A7
83	B69_L8_P	C9	84	B69_L23_P	A8

85	B69_L24_N	A11	86	B69_L19_N	C6
87	B69_L24_P	B11	88	B69_L19_P	C7
89	GND		90	GND	
91	B69_L16_N	D10	92	B69_L22_N	A10
93	B69_L16_P	D11	94	B69_L22_P	B10
95	B69_L18_N	C11	96	B69_L10_N	D9
97	B69_L18_P	D12	98	B69_L10_P	E9
99	GND		100	GND	
101	PS_MIO43	E30	102		
103	PS_MIO26	A29	104	PS_MIO32	B31
105	PS_MIO27	A30	106	PS_MIO35	C31
107	PS_MIO31	B30	108	PS_MIO36	C32
109	PS_MIO40	D31	110	PS_MIO37	C33
111	PS_MIO44	E32	112	PS_MIO29	A32
113	PS_MIO39	D30	114	PS_MIO30	A33
115	PS_MIO33	B33	116	PS_MIO34	B34
117	PS_MIO41	D32	118	PS_MIO42	D34
119	PS_MIO28	A31	120	PS_MIO38	C34

J30 Connector

The J30 connector carries the MGT transceiver signals from BANK505, some PS MIO pins, and I/O for BANK69. The I/O voltage standard for both the **BANK69** I/O and the **PS MIO** pins is 1.8V.

J30 Pin	Signal name	Pin Number	J30 Pin	Signal name	Pin Number
1	B69_L17_P	F12	2	SD_D2	F31
3	B69_L17_N	E12	4	SD_D3	F32
5	GND		6	GND	
7	B69_L12_N	F10	8	SD_CMD	F33
9	B69_L12_P	G10	10	SD_D0	E34
11	B69_L13_P	H11	12	SD_D1	F30
13	B69_L13_N	G11	14	SD_CLK	F34
15	GND		16	GND	
17	B69_L4_N	J11	18	SD_CD	E33
19	B69_L4_P	K12	20		
21	B69_L5_P	K14	22	USB_STP	H31
23	B69_L5_N	J14	24	USB_DIR	G30
25	GND		26	GND	
27	B69_L3_P	L12	28	USB_CLK	G29
29	B69_L3_N	L11	30	USB_NXT	G33
31			32	USB_DATA0	G34
33			34	USB_DATA1	H29
35	GND		36	GND	
37	B69_L2_N	J10	38	USB_DATA2	G31
39	B69_L2_P	K10	40	USB_DATA3	H32
41	B69_L1_N	L13	42	USB_DATA4	H33
43	B69_L1_P	M13	44	USB_DATA5	H34
45	GND		46	GND	
47			48	USB_DATA6	J29
49			50	USB_DATA7	J30
51			52	PHY1_TXD0	J32
53	VCC_3V3		54	PHY1_TXD1	J34
55	GND		56	GND	
57			58	PHY1_TXD2	K28

59			60	PHY1_TXD3	K29
61	PS_POR_B	M24	62	PHY1_TXCK	J31
63	FPGA_DONE	N24	64	PHY1_TXCTL	K30
65	GND		66	GND	
67	PS_MODE3	K25	68	PHY1_RXD3	L29
69	PS_MODE2	K26	70	PHY1_RXD2	K34
71	PS_MODE1	J26	72	PHY1_RXD1	K33
73	PS_MODE0	H27	74	PHY1_RXD0	K32
75	GND		76	GND	
77	FPGA_TCK	K27	78	PHY1_RXCTL	L30
79	FPGA_TDI	J27	80	PHY1_RXCK	K31
81	FPGA_TMS	H28	82	PHY1_MDC	L33
83	FPGA_TDO	G28	84	PHY1_MDIO	L34
85	GND		86	GND	
87	505_RX3_N	N34	88	505_TX3_N	N30
89	505_RX3_P	N33	90	505_TX3_P	N29
91	GND		92	GND	
93	505_RX2_N	R34	94	505_TX2_N	P32
95	505_RX2_P	R33	96	505_TX2_P	P31
97	GND		98	GND	
99	505_RX1_N	T32	100	505_TX1_N	R30
101	505_RX1_P	T31	102	505_TX1_P	R29
103	GND		104	GND	
105	505_RX0_N	U34	106	505_TX0_N	U30
107	505_RX0_P	U33	108	505_TX0_P	U29
109	GND		110	GND	
111	505_CLK0_N	T28	112	505_CLK1_N	P28
113	505_CLK0_P	T27	114	505_CLK1_P	P27
115	GND		116	GND	
117	505_CLK2_N	M28	118	505_CLK3_N	M32
119	505_CLK2_P	M27	120	505_CLK3_P	M31

J31 Connector

The J31 connector carries the I/O for **BANK64** and **BANK65**. The I/O voltage standard for these banks is **+1.8V**.

J31 PIN	Signal Name	PIN Number	J31 PIN	Signal Name	PIN Number
1	POWER_SW		2	VBAT_IN	Y23
3	B65_L24_N	AA20	4	B65_L2_N	AN19
5	B65_L24_P	AA19	6	B65_L2_P	AM19
7	B65_L13_N	AH23	8	B65_L18_N	AE24
9	B65_L13_P	AH22	10	B65_L18_P	AE23
11	GND		12	GND	
13	B65_L8_N	AL23	14	B65_L16_N	AG23
15	B65_L8_P	AL22	16	B65_L16_P	AF23
17	B65_L12_N	AJ22	18	B65_L3_N	AP22
19	B65_L12_P	AJ21	20	B65_L3_P	AP21
21	GND		22	GND	
23	B65_L5_N	AP23	24	B65_L7_N	AL21
25	B65_L5_P	AN22	26	B65_L7_P	AL20
27	B65_L10_N	AK23	28	B65_L21_N	AE20
29	B65_L10_P	AK22	30	B65_L21_P	AD20
31	GND		32	GND	

33	B65_L14_N	AH21	34	B65_L6_N	AN23
35	B65_L14_P	AG21	36	B65_L6_P	AM23
37	B65_L19_N	AE19	38	B65_L17_N	AF22
39	B65_L19_P	AE18	40	B65_L17_P	AF21
41	GND		42	GND	
43	B65_L15_N	AG20	44	B65_L4_N	AN21
45	B65_L15_P	AG19	46	B65_L4_P	AM21
47	B65_L20_N	AC19	48	B65_L11_N	AK20
49	B65_L20_P	AB19	50	B65_L11_P	AJ20
51	GND		52	GND	
53	B65_L23_N	AD19	54	B65_L1_N	AP20
55	B65_L23_P	AC18	56	B65_L1_P	AP19
57	B65_L22_N	AB18	58	B65_L9_N	AK19
59	B65_L22_P	AA18	60	B65_L9_P	AJ19
61	GND		62	GND	
63	B64_L1_P	AP18	64	B64_L9_P	AK18
65	B64_L1_N	AP17	66	B64_L9_N	AL18
67	B64_L6_P	AN17	68	B64_L14_P	AF18
69	B64_L6_N	AN16	70	B64_L14_N	AG18
71	GND		72	GND	
73	B64_L5_P	AP16	74	B64_L11_P	AJ17
75	B64_L5_N	AP15	76	B64_L11_N	AK17
77	B64_L3_P	AM18	78	B64_L4_P	AM14
79	B64_L3_N	AN18	80	B64_L4_N	AN14
81	GND		82	GND	
83	B64_L24_P	AD17	84	B64_L2_P	AN13
85	B64_L24_N	AD16	86	B64_L2_N	AP13
87	B64_L21_P	AB16	88	B64_L8_P	AL16
89	B64_L21_N	AB15	90	B64_L8_N	AL15
91	GND		92	GND	
93	B64_L7_P	AM16	94	B64_L12_P	AJ16
95	B64_L7_N	AM15	96	B64_L12_N	AJ15
97	B64_L10_P	AK15	98	B64_L16_P	AH14
99	B64_L10_N	AK14	100	B64_L16_N	AJ14
101	GND		102	GND	
103	B64_L20_P	AC17	104	B64_L15_P	AE17
105	B64_L20_N	AC16	106	B64_L15_N	AF17
107	B64_L18_P	AG15	108	B64_L17_P	AF16
109	B64_L18_N	AG14	110	B64_L17_N	AF15
111	GND		112	GND	
113	B64_L22_P	AA16	114	B64_L19_P	AD15
115	B64_L22_N	AA15	116	B64_L19_N	AE15
117	B64_L13_P	AH18	118	B64_L23_P	AA14
119	B64_L13_N	AH17	120	B64_L23_N	AB14

J32 Connector Pin Assignment

The J32 connector carries the transceiver signals for BANK223, BANK225, BANK226, and BANK227.

J31 PIN	Signal Name	PIN Number	J31 PIN	Signal Name	PIN Number
1	224_RX0_P	AP4	2	224_TX0_P	AN6
3	224_RX0_N	AP3	4	224_TX0_N	AN5
5	GND		6	GND	

7	224_RX1_P	AN2	8	224_TX1_P	AM4
9	224_RX1_N	AN1	10	224_TX1_N	AM3
11	GND		12	GND	
13	224_RX2_P	AL2	14	224_TX2_P	AL6
15	224_RX2_N	AL1	16	224_TX2_N	AL5
17	GND		18	GND	
19	224_RX3_P	AK4	20	224_TX3_P	AJ6
21	224_RX3_N	AK3	22	224_TX3_N	AJ5
23	GND		24	GND	
25	224_CLK1_P	AC10	26	224_CLK0_P	AD8
27	224_CLK1_N	AC9	28	224_CLK0_N	AD7
29	GND		30	GND	
31	225_RX0_P	AJ2	32	225_TX0_P	AH4
33	225_RX0_N	AJ1	34	225_TX0_N	AH3
35	GND		36	GND	
37	225_RX1_P	AG2	38	225_TX1_P	AG6
39	225_RX1_N	AG1	40	225_TX1_N	AG5
41	GND		42	GND	
43	225_RX2_P	AF4	44	225_TX2_P	AE6
45	225_RX2_N	AF3	46	225_TX2_N	AE5
47	GND		48	GND	
49	225_RX3_P	AE2	50	225_TX3_P	AD4
51	225_RX3_N	AE1	52	225_TX3_N	AD3
53	GND		54	GND	
55	225_CLK1_P	AA10	56	225_CLK0_P	AB8
57	225_CLK1_N	AA9	58	225_CLK0_N	AB7
59	GND		60	GND	
61	226_CLK1_P	W10	62	226_CLK0_P	Y8
63	226_CLK1_N	W9	64	226_CLK0_N	Y7
65	GND		66	GND	
67	226_RX1_P	AB4	68	226_RX0_P	AC2
69	226_RX1_N	AB3	70	226_RX0_N	AC1
71	GND		72	GND	
73	226_TX1_P	AA6	74	226_TX0_P	AC6
75	226_TX1_N	AA5	76	226_TX0_N	AC5
77	GND		78	GND	
79	226_RX2_P	AA2	80	226_RX3_P	W2
81	226_RX2_N	AA1	82	226_RX3_N	W1
83	GND		84	GND	
85	226_TX2_P	Y4	86	226_TX3_P	W6
87	226_TX2_N	Y3	88	226_TX3_N	W5
89	GND		90	GND	
91	227_CLK0_P	V8	92	227_CLK1_P	U10
93	227_CLK0_N	V7	94	227_CLK1_N	U9
95	GND		96	GND	
97	227_RX3_P	P4	98	227_TX3_P	N6
99	227_RX3_N	P3	100	227_TX3_N	N5
101	GND		102	GND	
103	227_RX2_P	R2	104	227_TX2_P	R6
105	227_RX2_N	R1	106	227_TX2_N	R5
107	GND		108	GND	
109	227_RX1_P	U2	110	227_TX1_P	T4

111	227_RX1_N	U1	112	227_TX1_N	T3
113	GND		114	GND	
115	227_RX0_P	V4	116	227_TX0_P	U6
117	227_RX0_N	V3	118	227_TX0_N	U5
119	GND		120	GND	