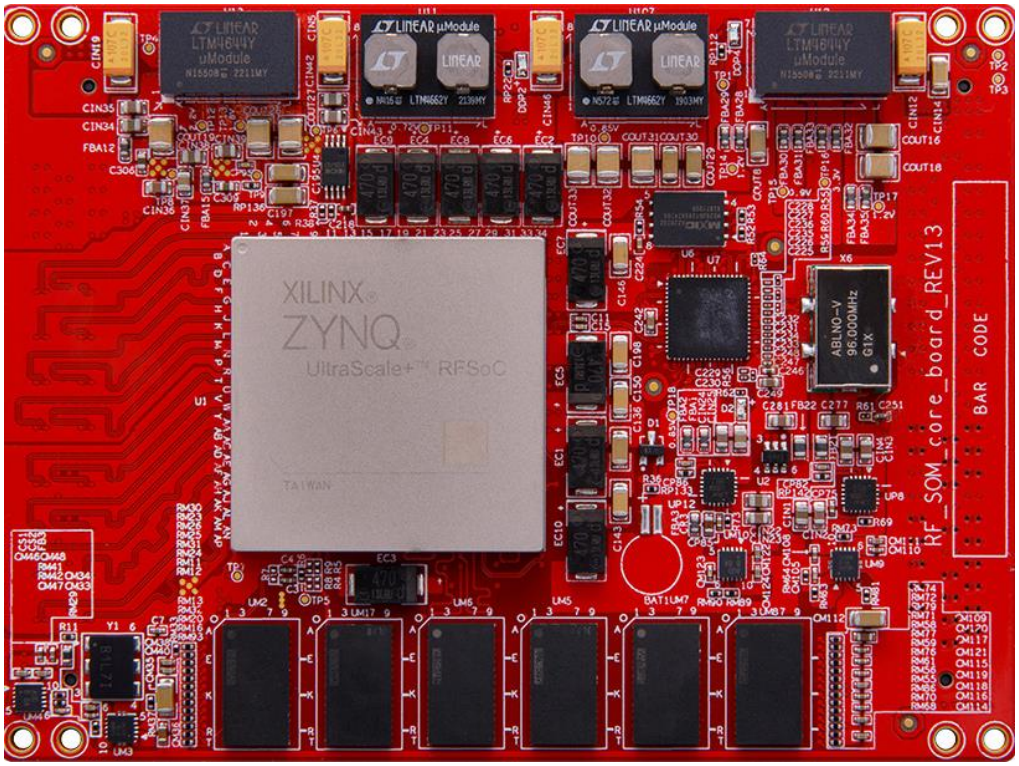
RFEVM development platform

ACRF47 User Manual

Rev. 1.0



Version Record

Version	Date	Release By	Description
Rev 1.0	2024/3/11	Kathy Xia	First Release

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Part 1: ACRF47 SOM Module

Part 1.1: Introduction

The ZYNQ chip of ACRF47 SOM module is based on Zynq UltraScale+ RFSoC Gen3 series ZU47DR-2FFVE1156I of XILINX.

This module uses six DDR4 chips MT40A512M16 from Micron, in which four DDR4 chips are mounted on the PS side to form a 64-bit data bus width and two pieces of DDR4 are mounted on the PL side to form a 32-bit data bus width. DDR4 capacity is 1GB per chip. DDR4 SDRAM can run up to 1200MHz (2400Mbps data rate). In addition, 1Gbit QSPI FLASH is also integrated on the module for boot storage configuration and system files.

To connect with the base board, the two 400Pin board-to-board connectors of this module expand the USB3.0 interface, Gigabit Ethernet interface, SD card interface, M.2 interface and the remaining MIO interface at the PS end, and expand four pairs of PS MGT high-speed transceiver interfaces; As well as 1 QSFP28 interface, 1 SFP interface and other IO at the PL end.

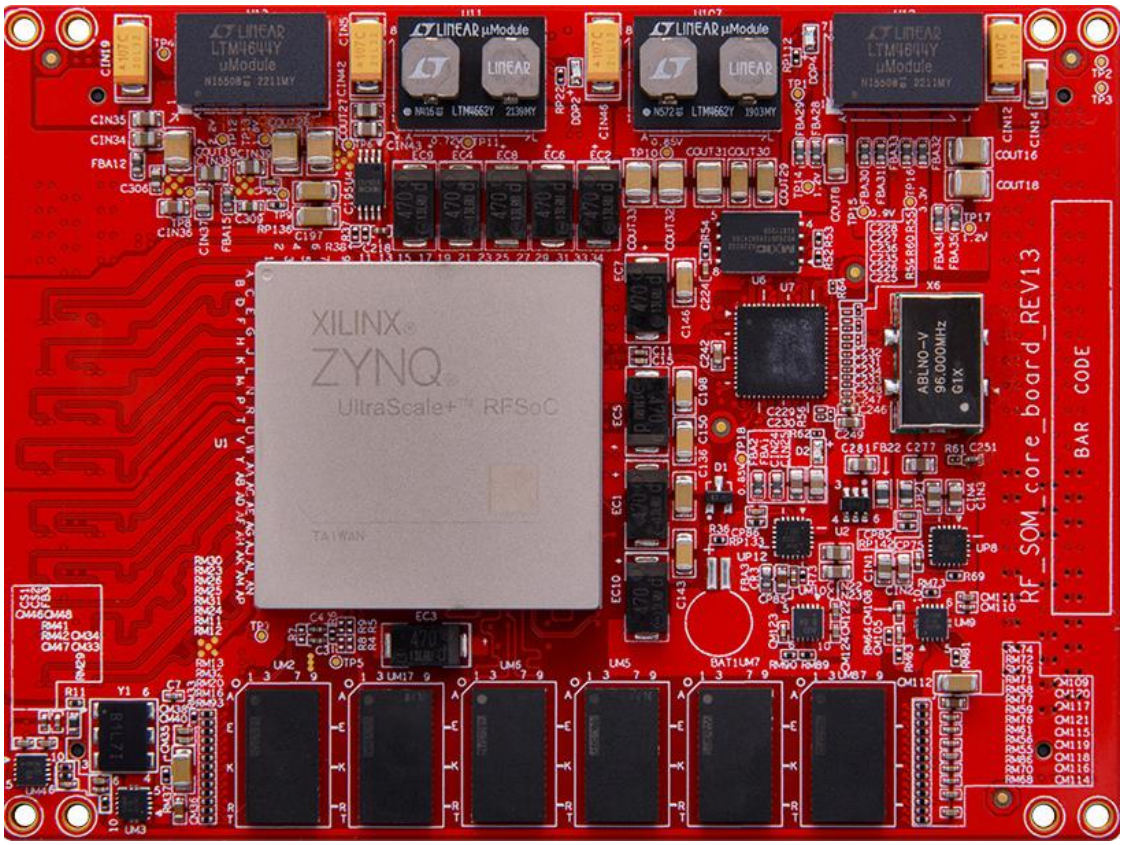

Figure 1: Front view of ACRF47 module

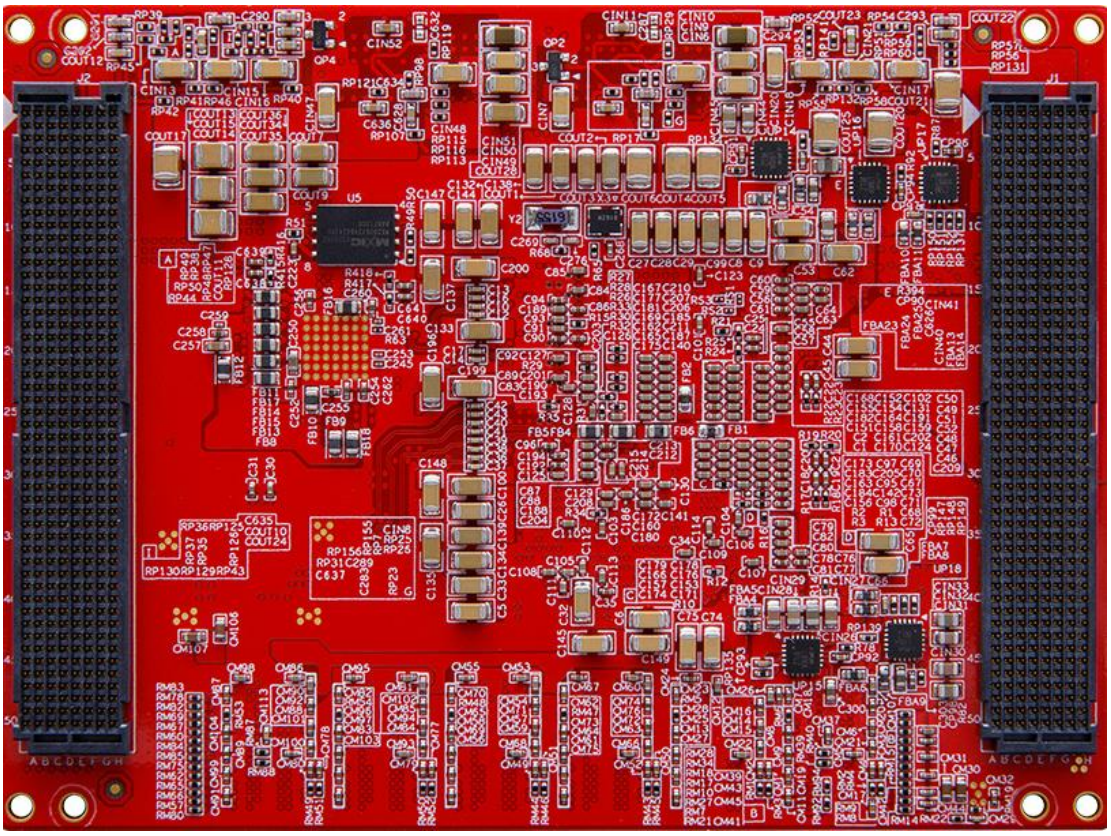

Figure 2: Back view of ACRF47 module

Part 1.2: Zynq Chip

The ACRF47 module uses a Zynq UltraScale+ RFSoC Gen3 series chip from Xilinx, model ZU47DR-2FFVE1156I. FPGA resources in the programmable logic section can provide high-throughput digital signal processing (DSP) and IP cores, such as digital up/down conversion (DUC/DDC) cores. FPGA acceleration is made easier by the software radio development architecture application programming interface and the FPGA infrastructure. This helps you get up and running quickly so you can focus on value-added IP. An FPGA system for common functions such as Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filters is a good place to start. You can then add your own IP blocks to the modular architecture using your preferred hardware description language (HDL). In addition to the FPGA architecture portion of the system, the Xilinx UltraScale+ RFSoC is equipped with four on-board application processing units (APUs) and two real-time processing units (RPUs). For applications that require an on-board embedded operating system for standalone operation.

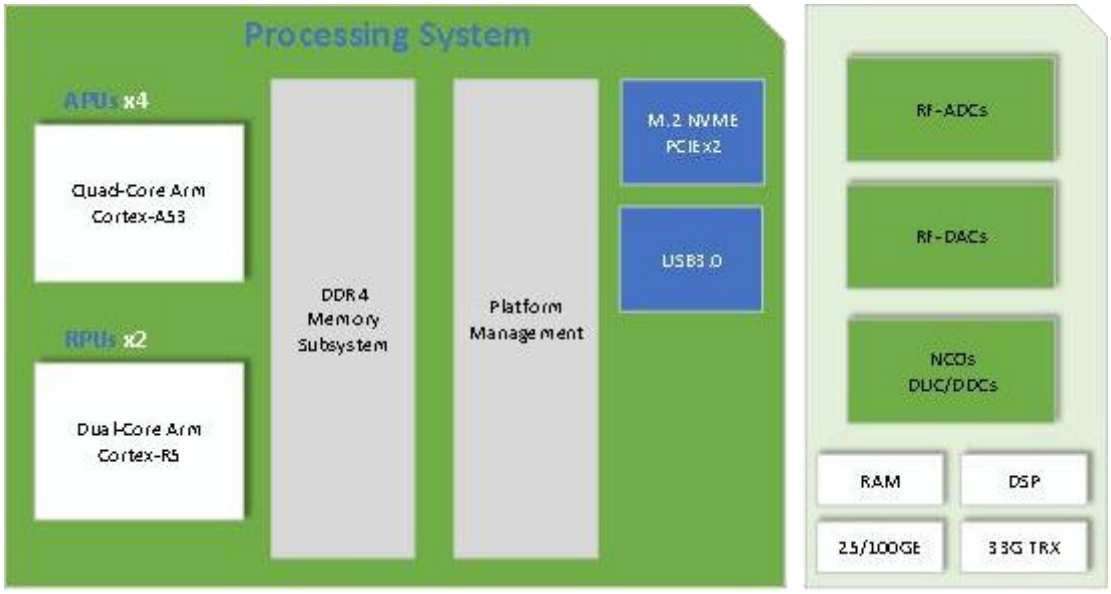

Figure 3: Block diagram of RFSOM hardware system

ACRF47 can support full differential extraction of AD/DA channels. Users can define RF conditioning circuits as required, support DC and AC coupling, and support PA \ LNA amplifier conditioning circuits. It can also support optional RF front-end, LO converter, duplexer, PA, LNA, etc.

Part 1.3: DDR4 SDRAM

The ACRF47 module is equipped with six Micron 1GB DDR4 chips, model MT40A512M16GE-083E, in which four DDR4 chips are mounted on the PS side, forming 64bit data bus bandwidth. Two pieces of DDR4 chips are mounted on the PL side to form 32bit data bus bandwidth. The maximum operating speed of DDR4 SDRAM on the PS side can reach 1200MHz (data rate 2400Mbps), and four DDR4 storage systems directly connected to the memory interface of the bank 504 of the PS. The maximum running speed of DDR SDRAM on the PL side can reach 1200MHz (data rate 2400Mbps), and two DDR4 chips are connected to the BANK65 and BANK66 interfaces of the FPGA. The specific configuration of PS-side and PL-side DDR4 SDRAM is shown in the following table.

Location	Tag number	Chip model	Capacity	Manufacturer
PS	UM5,UM6,UM7,UM8	MT40A512M16GE-083E	512x16bit	Micron
PL	UM1,UM2	MT40A512M16GE-083E	512x16bit	Micron

Table 1: DDR4 SDRAM Configuration

The hardware connection mode of DDR4 on the PS side is shown in figure 4:

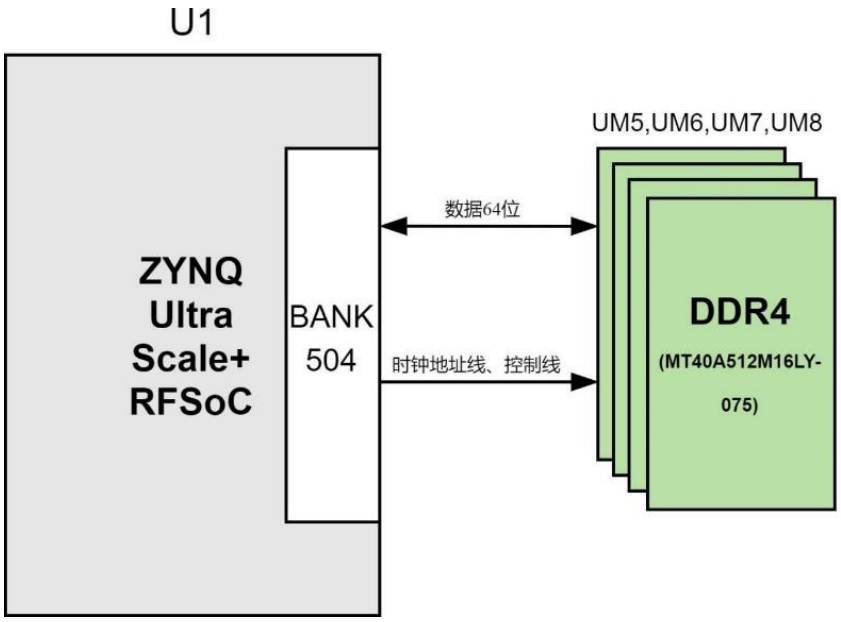

Figure 4: Schematic diagram of PS-side DDR4 SDRAM connection

The hardware connection mode of DDR4 SDRAM on the PL is shown in figure 5:

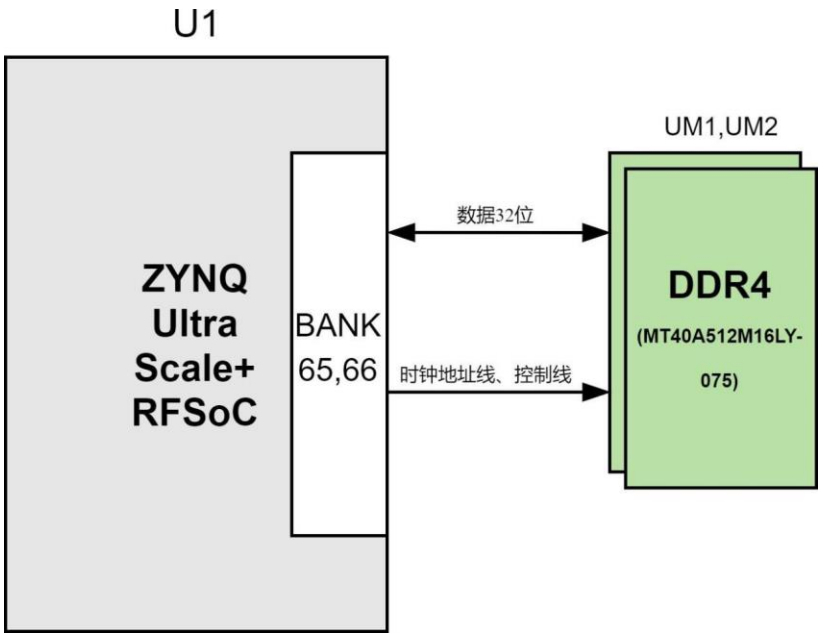

Figure 5: Schematic diagram of PL-side DDR4 SDRAM connection

Part 1.4: QSPI Flash

The ACRF47 module is equipped with two 512Mbit QUAD SPI FLASH chips to form an 8-bit bandwidth data bus. The FLASH model is MT25QU512ABBIEW9-0SIT, which uses 1.8V CMOS Voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code and its user data files. See the following table for the specific model and related features of QSPI Flash.

Location	Tag number	Chip model	Capacity	Manufacturer
PS	U5,U6	MT25QU512ABBIEW9-0SIT	512M bit	Micron

Table 2: QSPI Flash Models and Parameters

The QSPI FLASH is connected to the MIO of BANK500, the PS part of the ZYNQ chip. In the system design, it is necessary to configure these MIO functions of PS end as QSPI Flash interfaces.

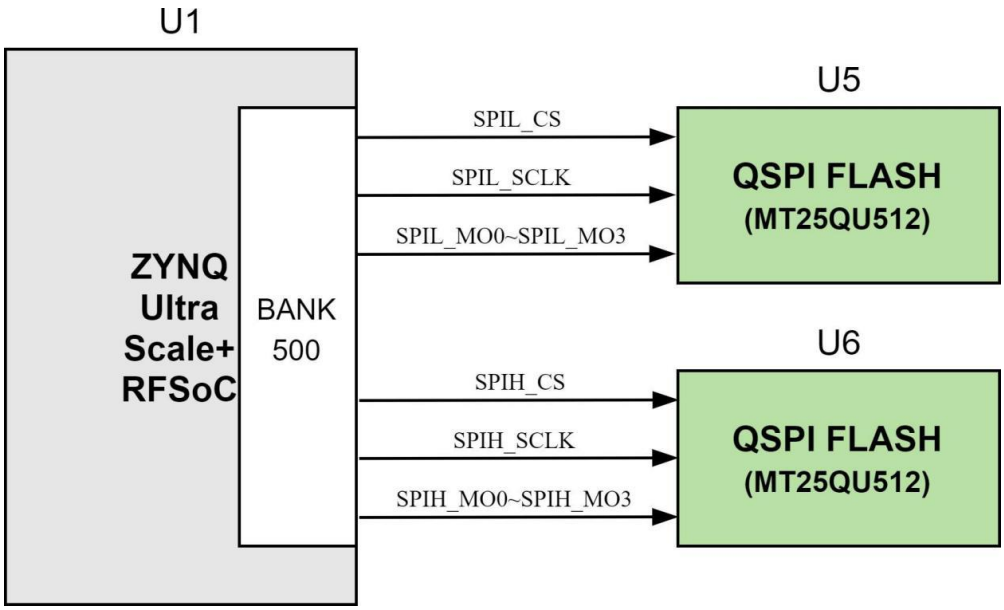

Figure 6: QSPI FLASH Connection Diagram

Signal name	Pin name	Pin number
SPIL_SCLK	PS_MIO0	J17
SPIL_MO1	PS_MIO1	J18
SPIL_MO2	PS_MIO2	J16
SPIL_MO3	PS_MIO3	K16
SPIL_MO0	PS_MIO4	G15
SPIL_CS	PS_MIO5	H18
SPIH_CS	PS_MIO7	K17
SPIH_MO0	PS_MIO8	E15
SPIH_MO1	PS_MIO9	F15
SPIH_MO2	PS_MIO10	C15
SPIH_MO3	PS_MIO11	G16
SPIH_SCLK	PS_MIO12	B15

Table 3: Configuring Chip Pin Assignments

Part 1.5: EEPROM

The ACRF47 module has an EEPROM on board, the model is AT24CM01, the capacity is 1Mbit, and it is connected to the PS end for communication through the IIC bus.

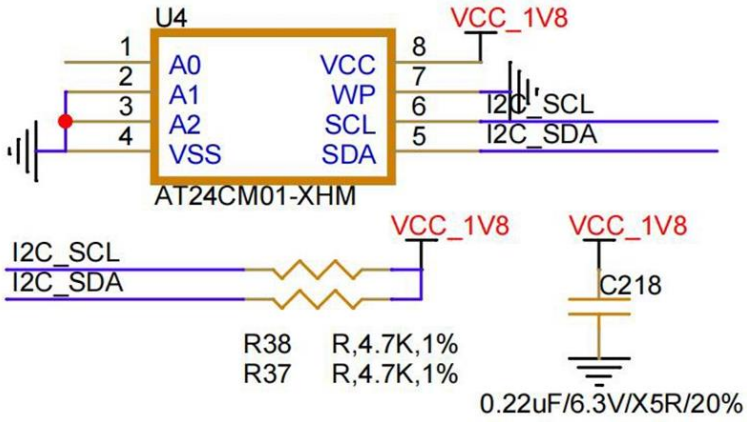

Figure 7: EEPROM Hardware Schematic

Signal name	Pin name	Pin number	Remark
IIC_SDA	PS_MIO25	B17	I2C Data Signal
IIC_SCL	PS_MIO24	A17	I2C Clock Signal

Table 4: EEPROM Pin Assignment

Part 1.6: Clock Configuration

Dual crystal oscillator clock is provided on SOM module. The system clock uses 33.3333MHz active crystal oscillator by default. The package is 3.2x2.5mm. Crystal 32.768 KHz, driving the ACRF47 internal RTC circuit. The schematic diagram of the clock circuit design is shown in the following figure:

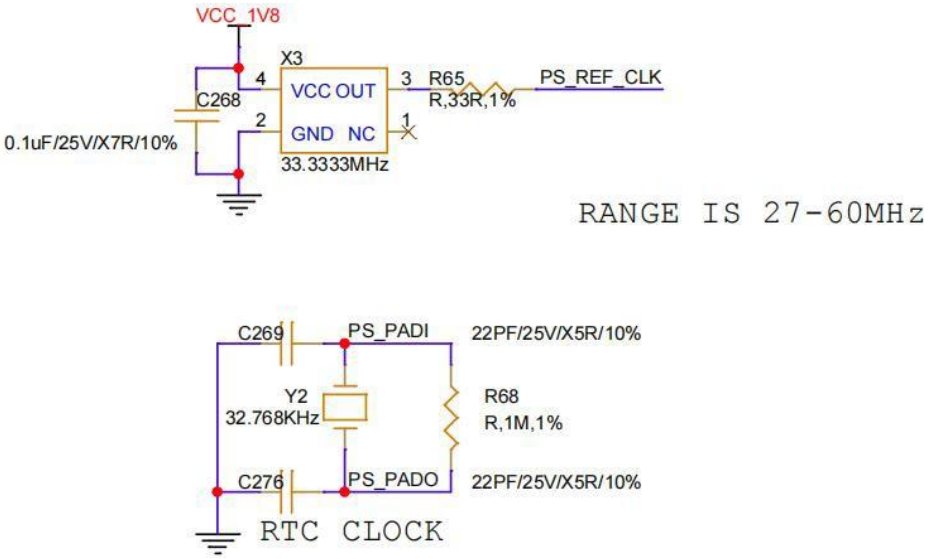

Figure 8: Schematic diagram of crystal oscillator

The module system uses LMK04828 clock chip to distribute the clock required by each module, and the main crystal oscillator uses 19.2MHz high stability OCXO. Support GTY recovery clock, support input of external reference clock and SYSREF input, and realize parallel connection of multiple modules to form a larger-scale coherent RF channel.

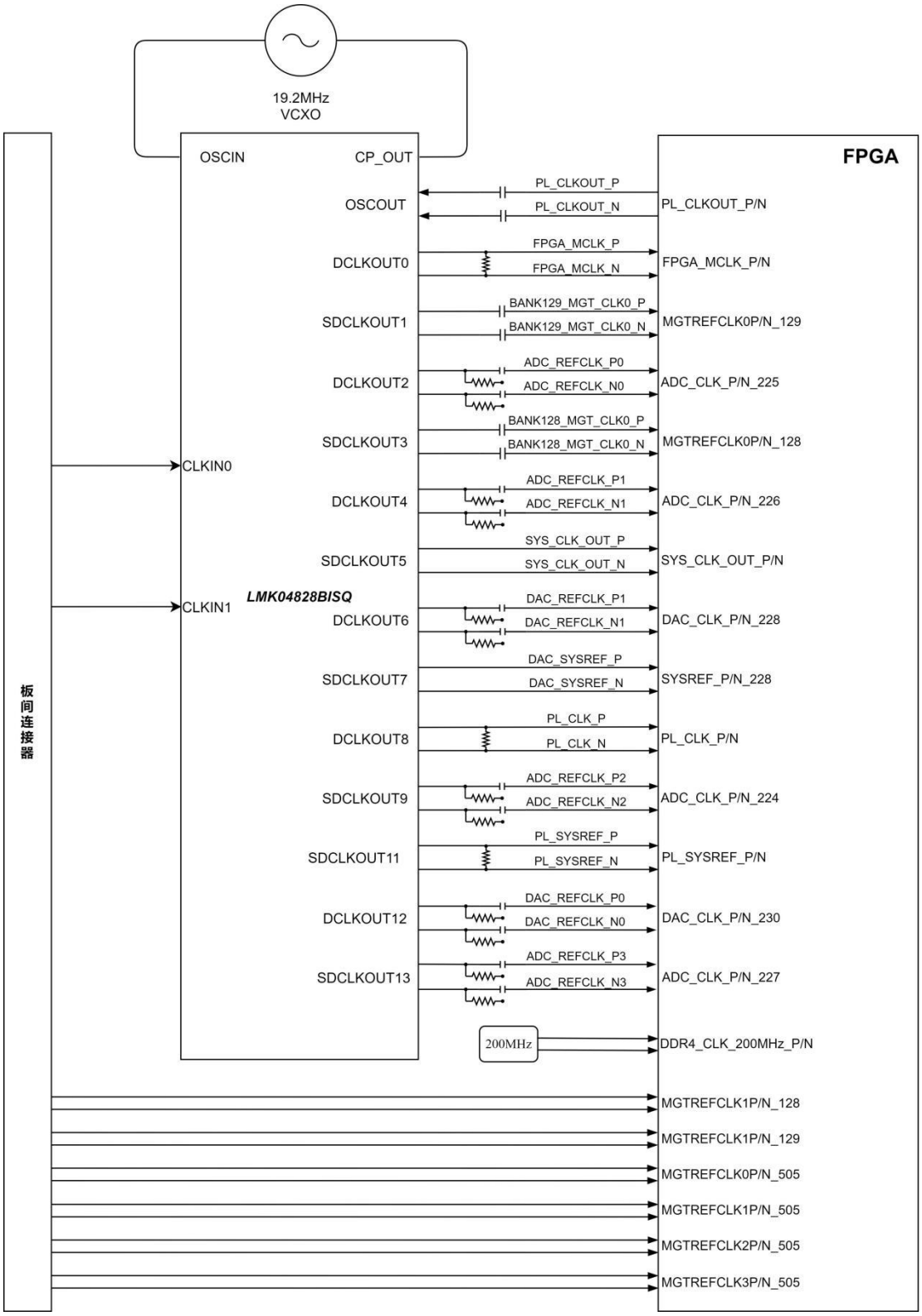

Figure 9: Schematic diagram of clock distribution connection

Part 1.7: PS-GTR Interface

The PS-side GTR high-speed BANK of the ACRF47 module is not used and is pulled out through the connector. It supports a data rate of up to 6.0 Gb/s and can be used as x1, x2 and x4 of PCIE Gen2. As well as can also be used as a SATA interface, supporting 1.5Gb/s, 3.0Gb/s, 6Gb/s data rates, and DP interface and USB3.0 interface and other applications.

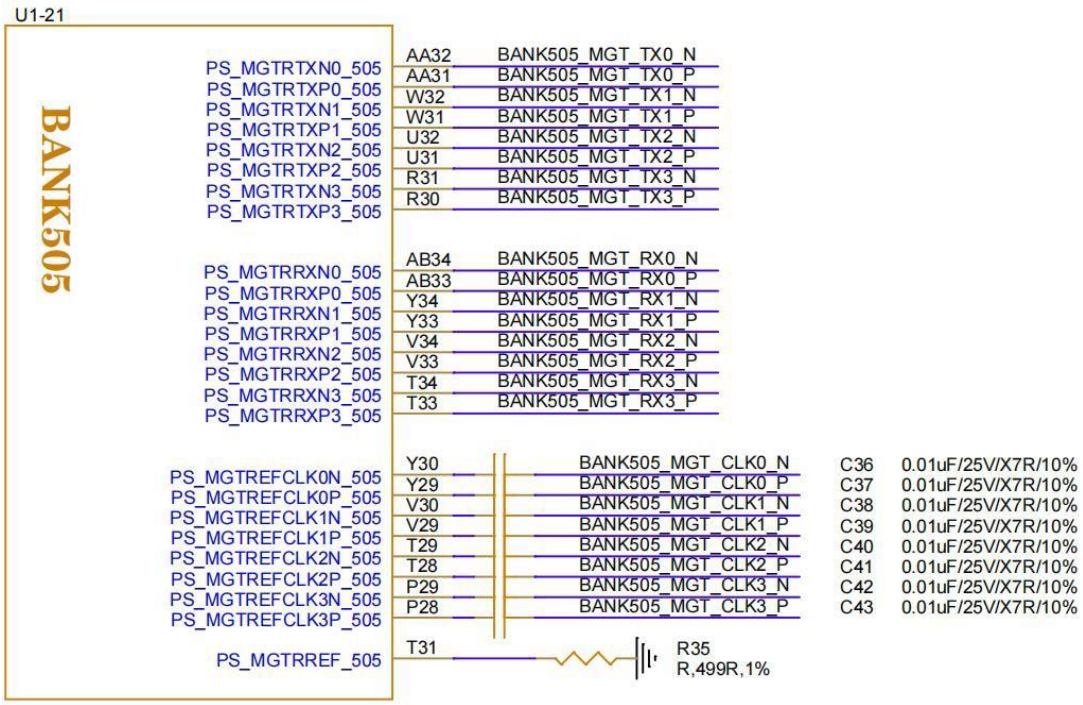

Figure 10: Mapping Diagram of GTR High-speed Transceiver at PS End

Part 1.8: PCIE Gen4 Connector (Requires PCIe carrier card)

The ACRF47 supports the GTY high-speed transceiver, which enables PCIe x8 Gen4.0 at data rates up to 16.0 Gb/s, as well as 100G optical interface interconnects. It is convenient for users to develop for the second time, and the design risk is small, convenient, and flexible.

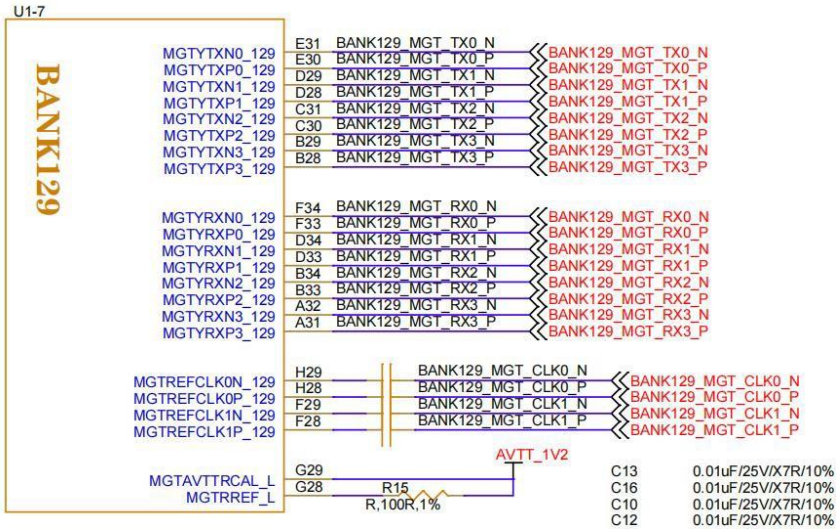

Figure 11: High Speed Transceiver Map

Part 1.9: RF-ADC Interface

The FPGA chip used in the ACRF47 module is the only single-chip adaptive radio platform of Zynq UltraScale+ RFSoC Gen3 series in the industry, which integrates a 14-bit RF-ADC. The maximum sampling rate is up to 5GSPS, and the VCM signal is also brought out to the connector, making it easier for the user to adjust the common-mode voltage.

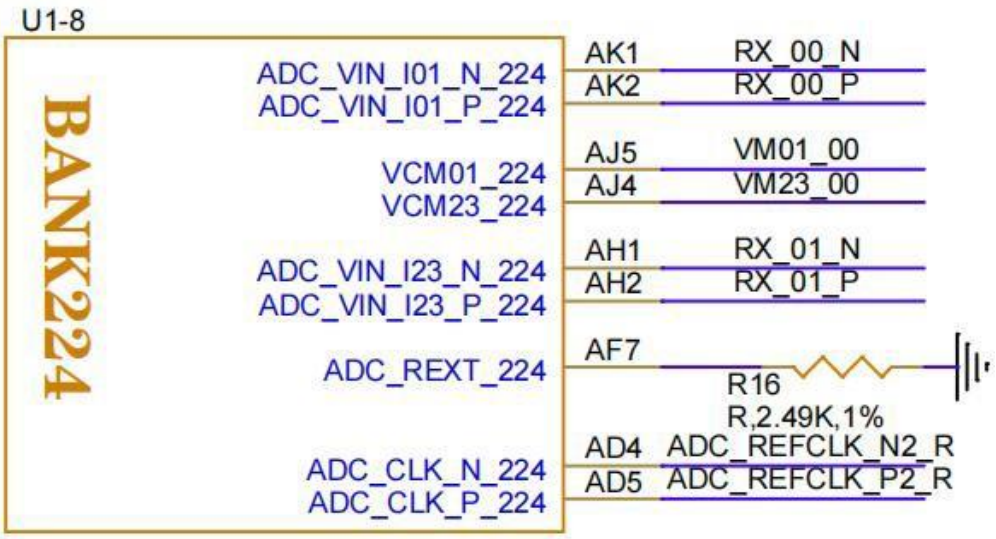

Figure 12: RF-to-ADC Interface Schematic

Part 1.10: RF-DAC Interface

The FPGA chip used in the core module of ACRF47 is the only single-chip adaptive radio platform of Zynq UltraScale+ RFSoC Gen3 series in the industry. The chip integrates a 14-bit RF-DAC with a maximum sampling rate of 9.85 GSPS.

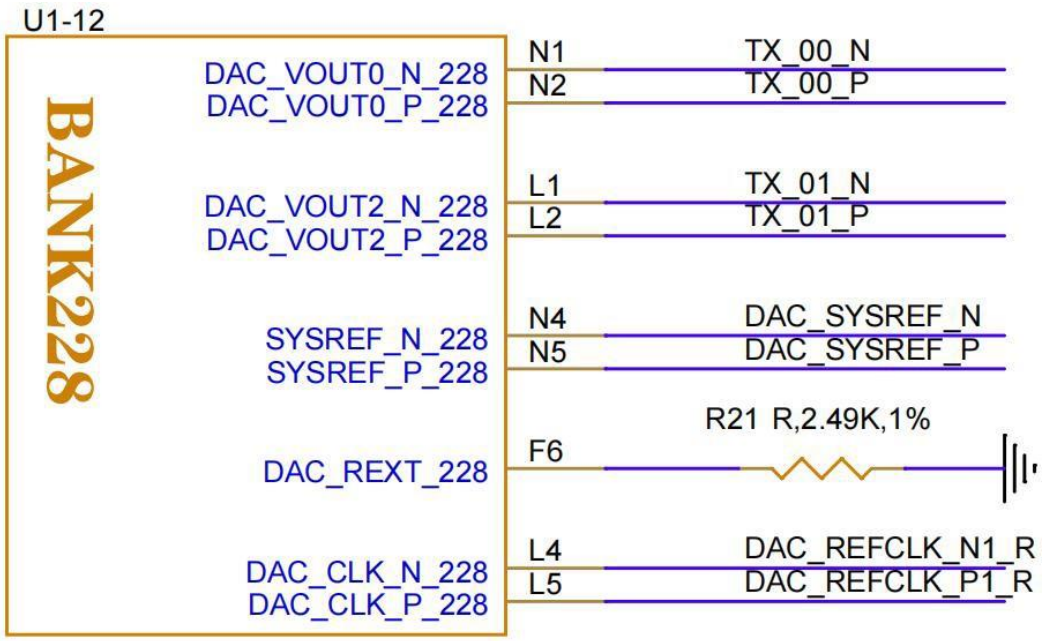

Figure 13: RF-to-DAC Interface Schematic

Part 1.11: Power Source

The ACRF47 module is powered by DC 5V, and the power is supplied to the module through the connector in base board. The ACRF47 module typically consumes 60W. The 5V system power supply drives the FPGA and other circuits on the board by converting different voltages through the buck regulator. The power supply of the ADC and DAC on the board is provided by the linear low-voltage LDO, which has good power supply rejection (PSRR).

The extended IO BANK interface level of the core module is shown in the figure below:

BANK	Level (V)	Remark
BANK89	Supplied from the base board	HD _ BANK supports 1.2 ~ 3.3V (HD I/O only) at ± 5%
BANK128	MGTY	PCIE Gen4 signal
BANK129	MGTY	PCIE Gen4 signal
BANK501	Supplied from the base board	MIO BANK supports 1.8V, 2.5V, and 3.3V at ± 5%
BANK502	Supplied from the base board	MIO BANK supports 1.8V, 2.5V, and 3.3V at ± 5%
BANK503	1.8 V fixed	Configure pin output, mode selection, system reset signal
BANK505	PS_MGTR	Without any definition, the high-speed signal pin and clock signal are all pulled out to the connector.

Table 5: Extended IO BANK interface level of the core module

The power supply design block diagram of the ACRF47 core module is shown below:

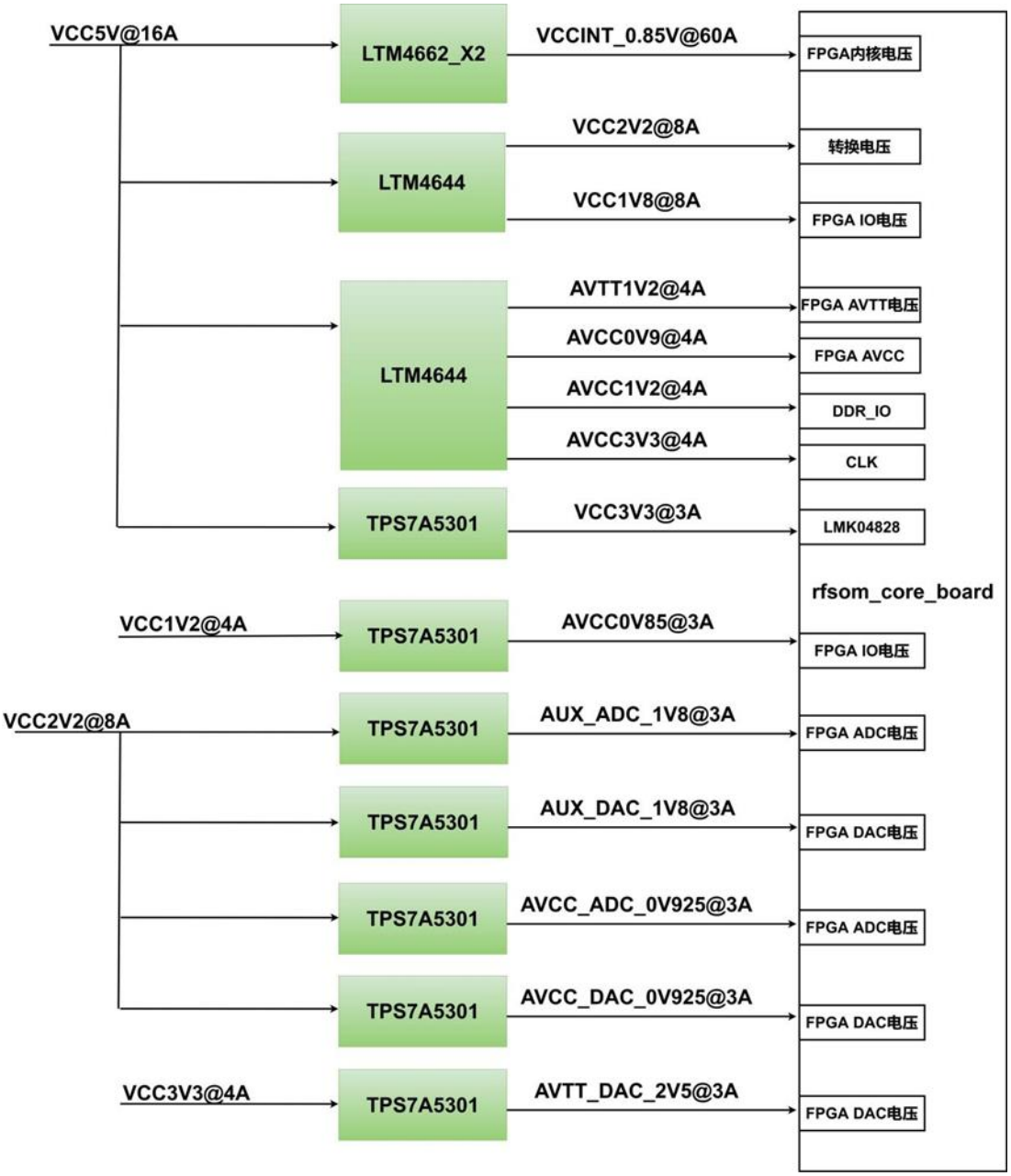

Figure 14: Design block diagram of ACRF47 module power supply

Part 1.12: Structure Diagram

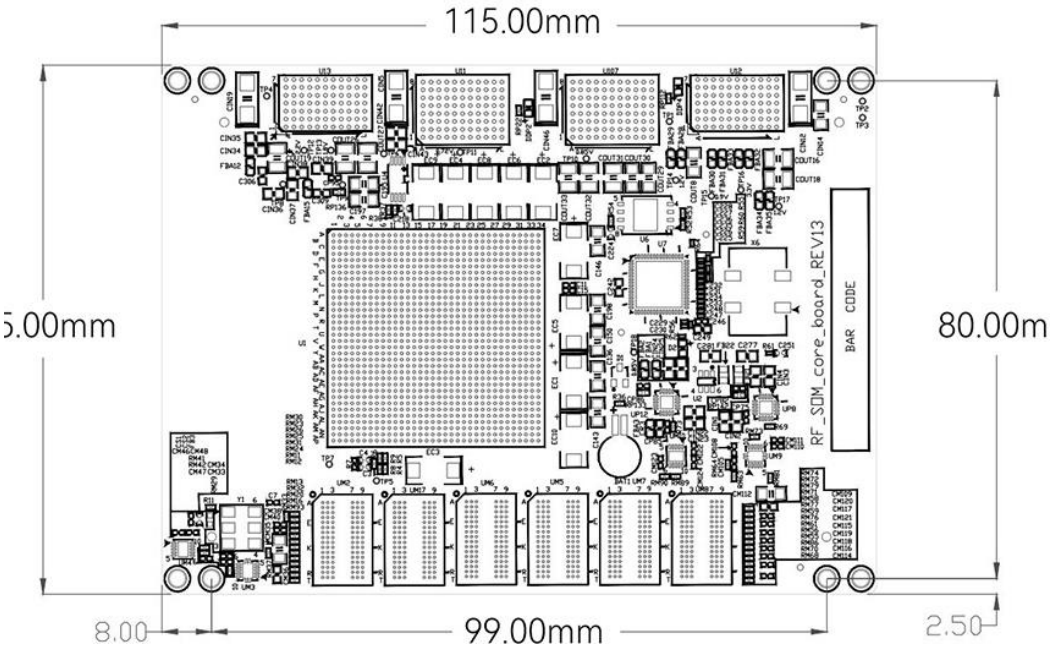

Figure 15: Front view of ACRF47 core module

Part 1.13: Connector Pin Definition

Two high-speed expansion ports are extended on the module, and two 400Pin inter-board connectors (J1, J2) are used to connect with the base board. The connector is the LPAM_50_01_0_L_08_2_K_TR connector of Samtec.

The connector signals are defined as follows:

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
A1	GND	B1	VCC_5V	C1	VCC_5V	D1	VCC_5V
A2	GND	B2	VCC_5V	C2	VCC_5V	D2	VCC_5V
A3	GND	B3	GND	C3	GND	D3	GND
A4	GND	B4	GND	C4	GND	D4	GND
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	GND	C6	GND	D6	GND
A7	GND	B7	BANK89_IO_L1P	C7	BANK89_IO_L1N	D7	GND
A8	GND	B8	GND	C8	GND	D8	BANK89_IO_L2P

A9	GND	B9	BANK89_IO_L3P	C9	BANK89_IO_L3N	D9	GND
A10	GND	B10	GND	C10	GND	D10	BANK89_IO_GC_L5P
A11	GND	B11	BANK89_IO_GC_L7P	C11	BANK89_IO_GC_L7N	D11	GND
A12	GND	B12	GND	C12	GND	D12	BANK89_IO_GC_L6P
A13	GND	B13	BANK89_IO_L4P	C13	BANK89_IO_L4N	D13	GND
A14	GND	B14	GND	C14	GND	D14	BANK89_IO_L9P
A15	GND	B15	GND	C15	GND	D15	GND
A16	GND	B16	GND	C16	GND	D16	GND
A17	GND	B17	GND	C17	GND	D17	GND
A18	GND	B18	TX_06_P	C18	TX_06_N	D18	GND
A19	GND	B19	GND	C19	GND	D19	GND
A20	GND	B20	GND	C20	GND	D20	GND
A21	GND	B21	GND	C21	GND	D21	GND
A22	GND	B22	TX_04_P	C22	TX_04_N	D22	GND
A23	GND	B23	GND	C23	GND	D23	GND
A24	GND	B24	GND	C24	GND	D24	GND
A25	GND	B25	GND	C25	GND	D25	GND
A26	GND	B26	TX_02_P	C26	TX_02_N	D26	GND
A27	GND	B27	GND	C27	GND	D27	GND
A28	GND	B28	GND	C28	GND	D28	GND
A29	GND	B29	GND	C29	GND	D29	GND
A30	GND	B30	TX_00_P	C30	TX_00_N	D30	GND
A31	GND	B31	GND	C31	GND	D31	GND
A32	GND	B32	GND	C32	GND	D32	GND
A33	GND	B33	GND	C33	GND	D33	NC
A34	GND	B34	RX_06_P	C34	RX_06_N	D34	GND
A35	GND	B35	GND	C35	GND	D35	GND

A36	GND	B36	GND	C36	GND	D36	GND
A37	GND	B37	GND	C37	GND	D37	NC
A38	GND	B38	RX_04_P	C38	RX_04_N	D38	GND
A39	GND	B39	GND	C39	GND	D39	GND
A40	GND	B40	GND	C40	GND	D40	GND
A41	GND	B41	GND	C41	GND	D41	NC
A42	GND	B42	RX_02_P	C42	RX_02_N	D42	GND
A43	GND	B43	GND	C43	GND	D43	GND
A44	GND	B44	GND	C44	GND	D44	GND
A45	GND	B45	GND	C45	GND	D45	NC
A46	GND	B46	RX_00_P	C46	RX_00_N	D46	GND
A47	GND	B47	GND	C47	GND	D47	GND
A48	GND	B48	GND	C48	GND	D48	GND
A49	GND	B49	GND	C49	GND	D49	GND
A50	GND	B50	GND	C50	GND	D50	GND

Table 5: Signal Definition of J1 Connector

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
E1	VCC_5V	F1	VCC_5V	G1	VCC_5V	H1	GND
E2	VCC_5V	F2	VCC_5V	G2	VCC_5V	H2	GND
E3	GND	F3	GND	G3	GND	H3	GND
E4	GND	F4	GND	G4	GND	H4	GND
E5	GND	F5	GND	G5	GND	H5	GND
E6	GND	F6	GND	G6	GND	H6	GND
E7	GND	F7	BANK89_IO_L12P	G7	BANK89_IO_L12N	H7	GND
E8	BANK89_IO_L2N	F8	GND	G8	GND	H8	GND
E9	GND	F9	BANK89_IO_GC_L8P	G9	BANK89_IO_GC_L8N	H9	GND
E10	BANK89_IO_GC_L5N	F10	GND	G10	GND	H10	GND

E11	GND	F11	BANK89_IO_L10P	G11	BANK89_IO_L10N	H11	GND
E12	BANK89_IO_GC_L6N	F12	GND	G12	GND	H12	GND
E13	GND	F13	BANK89_IO_L11P	G13	BANK89_IO_L11N	H13	GND
E14	BANK89_IO_L9N	F14	GND	G14	GND	H14	GND
E15	GND	F15	GND	G15	GND	H15	GND
E16	GND	F16	GND	G16	GND	H16	GND
E17	GND	F17	GND	G17	GND	H17	GND
E18	GND	F18	TX_07_P	G18	TX_07_N	H18	GND
E19	GND	F19	GND	G19	GND	H19	GND
E20	GND	F20	GND	G20	GND	H20	GND
E21	GND	F21	GND	G21	GND	H21	GND
E22	GND	F22	TX_05_P	G22	TX_05_N	H22	GND
E23	GND	F23	GND	G23	GND	H23	GND
E24	GND	F24	GND	G24	GND	H24	GND
E25	GND	F25	GND	G25	GND	H25	GND
E26	GND	F26	TX_03_P	G26	TX_03_N	H26	GND
E27	GND	F27	GND	G27	GND	H27	GND
E28	GND	F28	GND	G28	GND	H28	GND
E29	GND	F29	GND	G29	GND	H29	GND
E30	GND	F30	TX_01_P	G30	TX_01_N	H30	GND
E31	GND	F31	GND	G31	GND	H31	GND
E32	GND	F32	GND	G32	GND	H32	GND
E33	GND	F33	GND	G33	GND	H33	GND
E34	GND	F34	RX_07_P	G34	RX_07_N	H34	GND
E35	NC	F35	GND	G35	GND	H35	GND
E36	GND	F36	GND	G36	GND	H36	GND
E37	GND	F37	GND	G37	GND	H37	GND
E38	GND	F38	RX_05_P	G38	RX_05_N	H38	GND

E39	NC	F39	GND	G39	GND	H39	GND
E40	GND	F40	GND	G40	GND	H40	GND
E41	GND	F41	GND	G41	GND	H41	GND
E42	GND	F42	RX_03_P	G42	RX_03_N	H42	GND
E43	NC	F43	GND	G43	GND	H43	GND
E44	GND	F44	GND	G44	GND	H44	GND
E45	GND	F45	GND	G45	GND	H45	GND
E46	GND	F46	RX_01_P	G46	RX_01_N	H46	GND
E47	NC	F47	GND	G47	GND	H47	GND
E48	GND	F48	GND	G48	GND	H48	GND
E49	GND	F49	GND	G49	GND	H49	GND
E50	GND	F50	GND	G50	GND	H50	GND

Table 6: J1 Connector Signal Definition

Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network	Mark Number	Signal Network
E1	VCCO_501	F1	VCC_5V	G1	VCC_5V	H1	GND
E2	VCCO_501	F2	VCC_501	G2	VCC_5V	H2	GND
E3	GND	F3	GND	G3	GND	H3	GND
E4	GND	F4	CLKIN0_P	G4	CLKIN0_N	H4	GND
E5	SYSREF_IN_N	F5	GND	G5	GND	H5	GND
E6	GND	F6	GND	G6	GND	H6	GND
E7	GND	F7	BANK501_PS_MIO37	G7	BANK501_PS_MIO34	H7	GND
E8	BANK501_PS_MIO36	F8	GND	G8	GND	H8	GND
E9	GND	F9	BANK501_PS_MIO41	G9	BANK501_PS_MIO38	H9	GND
E10	BANK501_PS_MIO39	F10	GND	G10	GND	H10	GND
E11	GND	F11	BANK501_PS_MIO43	G11	BANK501_PS_MIO44	H11	GND
E12	BANK501_PS_MIO45	F12	GND	G12	GND	H12	GND

E13	GND	F13	BANK501_PS_MIO48	G13	BANK501_PS_MIO51	H13	GND
E14	BANK501_PS_MIO47	F14	GND	G14	GND	H14	GND
E15	GND	F15	BANK501_PS_MIO58	G15	BANK501_PS_MIO60	H15	GND
E16	BANK501_PS_MIO59	F16	GND	G16	GND	H16	GND
E17	GND	F17	BANK501_PS_MIO63	G17	BANK501_PS_MIO62	H17	GND
E18	BANK501_PS_MIO55	F18	GND	G18	GND	H18	GND
E19	GND	F19	BANK501_PS_MIO64	G19	BANK501_PS_MIO65	H19	GND
E20	BANK501_PS_MIO71	F20	GND	G20	GND	H20	GND
E21	GND	F21	BANK501_PS_MIO75	G21	BANK501_PS_MIO70	H21	GND
E22	BANK501_PS_MIO74	F22	GND	G22	GND	H22	GND
E23	GND	F23	JTAG_TDI	G23	PS_ERROR	H23	GND
E24	BANK501_PS_MIO77	F24	GND	G24	GND	H24	GND
E25	GND	F25	PS_MODE2	G25	PS_MODE0	H25	GND
E26	PS_MODE1	F26	GND	G26	GND	H26	GND
E27	GND	F27	NC	G27	NC	H27	GND
E28	JTAG_TCK	F28	GND	G28	GND	H28	GND
E29	GND	F29	BANK129_MGT_RX1_P	G29	BANK129_MGT_RX1_N	H29	GND
E30	BANK129_MGT_RX2_N	F30	GND	G30	GND	H30	GND
E31	GND	F31	BANK129_MGT_TX2_P	G31	BANK129_MGT_TX2_N	H31	GND
E32	BANK129_MGT_TX3_N	F32	GND	G32	GND	H32	GND
E33	GND	F33	BANK505_MGT_CLK0_P	G33	BANK505_MGT_CLK0_N	H33	GND
E34	BANK129_MGT_TX0_N	F34	GND	G34	GND	H34	GND
E35	GND	F35	BANK505_MGT_CLK3_P	G35	BANK505_MGT_CLK3_N	H35	GND
E36	BANK505_MGT_CLK2_N	F36	GND	G36	GND	H36	GND
E37	GND	F37	BANK128_MGT_RX1_P	G37	BANK128_MGT_RX1_N	H37	GND

E38	BANK128_MGT_RX2_N	F38	GND	G38	GND	H38	GND
E39	GND	F39	BANK128_MGT_TX2_P	G39	BANK128_MGT_TX2_N	H39	GND
E40	BANK128_MGT_CLK1_N	F40	GND	G40	GND	H40	GND
E41	GND	F41	BANK128_MGT_TX0_P	G41	BANK128_MGT_TX0_N	H41	GND
E42	BANK128_MGT_TX1_N	F42	GND	G42	GND	H42	GND
E43	GND	F43	BANK505_MGT_TX2_P	G43	BANK505_MGT_TX2_N	H43	GND
E44	BANK505_MGT_TX1_N	F44	GND	G44	GND	H44	GND
E45	GND	F45	BANK505_MGT_RX2_P	G45	BANK505_MGT_RX2_N	H45	GND
E46	BANK505_MGT_RX3_N	F46	GND	G46	GND	H46	GND
E47	GND	F47	BANK129_MGT_CLK1_N	G47	BANK129_MGT_CLK1_P	H47	GND
E48	BANK505_MGT_RX0_N	F48	GND	G48	GND	H48	GND
E49	GND	F49	GND	G49	GND	H49	GND
E50	GND	F50	GND	G50	GND	H50	GND

Table 7: Definition of J2 connector signal