AMD FPGA

AC7Z045 SoM

User Manual

ALINX

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Overview

Alinx Electronic Limited has officially released the 2025 model of the SoM (System on Module based on the AMD ZYNQ7000 platform, model AC7Z045. We have prepared this user manual to help you quickly understand this development platform.

The AC7Z045 SoM (System on Module) employs the AMD Zynq7000 SoC chip solution, model XC7Z045, integrating dual-core ARM Cortex-A9 processors and FPGA programmable logic into a single chip. The SoM includes 4 pieces totaling 2GB of high-speed DDR3 SDRAM, one 8GB eMMC storage chip, and two 256Mb QSPI FLASH chips.

1 SoM Introduction

1.1 AX7Z045 SoM

Introduction

The AC7Z045 SoM (System on Module) features the AMD ZYNQ7000 series chip, model XC7Z045-2FFG900. The PS system of the ZYNQ chip integrates two ARM Cortex™-A9 processors, an AMBA® interconnect, internal memory, external memory interfaces, and peripherals. The FPGA portion of the ZYNQ chip is rich in programmable logic units, DSP slices, and internal RAM.

This SoM utilizes four Micron 512MB DDR3 memory chips model MT41J256M16HA-125, providing a total capacity of 2GB. Two chips are connected to each of the PS and PL sides, forming 32-bit bus widths. The DDR3 SDRAM on the PS side can operate at a maximum speed of 533MHz (data rate of 1066Mbps), while on the PL side, it can reach up to 800MHz (data rate of 1600Mbps). The SoM also incorporates two 256Mbit QSPI FLASH chips and one 8GB eMMC FLASH chip for boot storage configuration and system files.

For interfacing with the baseboard, this SoM extends four board-to-board connectors from the PS side, including USB interfaces, gigabit Ethernet interfaces, an SD card slot, and other remaining MIO ports. It also extends 16 pairs of high-speed GTX transceiver interfaces from the ZYNQ chip, as well as almost all IO ports from the PL side (140 3.3V IOs and 48 1.8V IOs). The IO voltage levels of BANK10, BANK11, and BANK12 can be modified by changing the LDO chips on the SoM, catering to different voltage interface

requirements. This makes the SoM an excellent choice for users needing a substantial number of IOs. Additionally, the routing from the ZYNQ chip to the interfaces is managed for equal length and differential signals, and the SoM's dimensions are only 80x60mm, making it highly suitable for secondary development.

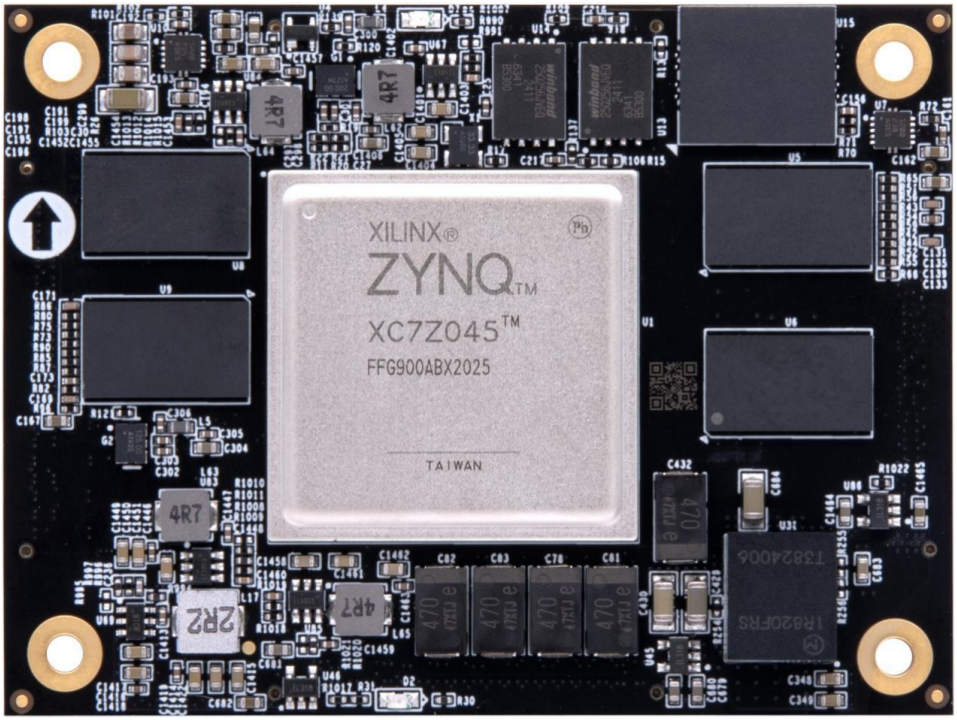

Figure 3: AC7Z045 SoM Front View

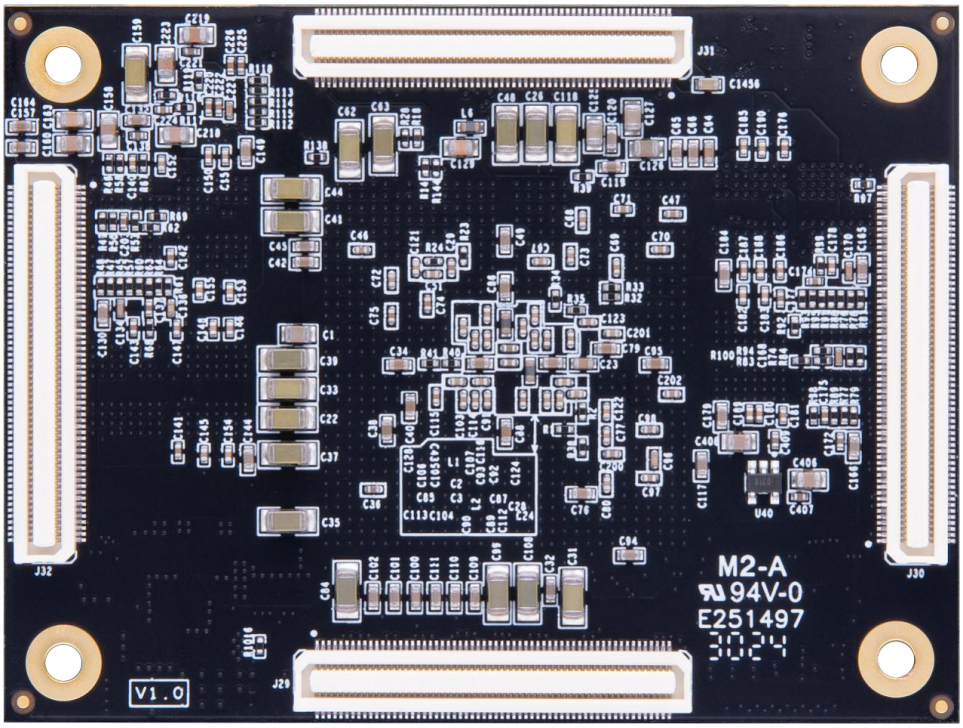

Figure 4: AC7Z045 SoM Back View

ZYNQ Chip

The SoM (System on Module) employs the AMD Zynq7000 series chip, model XC7Z045-2FFG900i. The PS (Processing System) of the chip integrates two ARM Cortex™ -A9 processors, AMBA® interconnect, internal memory, external memory interfaces, and peripherals. These peripherals primarily include USB bus interfaces, Ethernet interfaces, SD/SDIO interfaces, I2C bus interfaces, CAN bus interfaces, UART interfaces, and GPIO. The PS can operate independently and will boot upon power-up or reset.

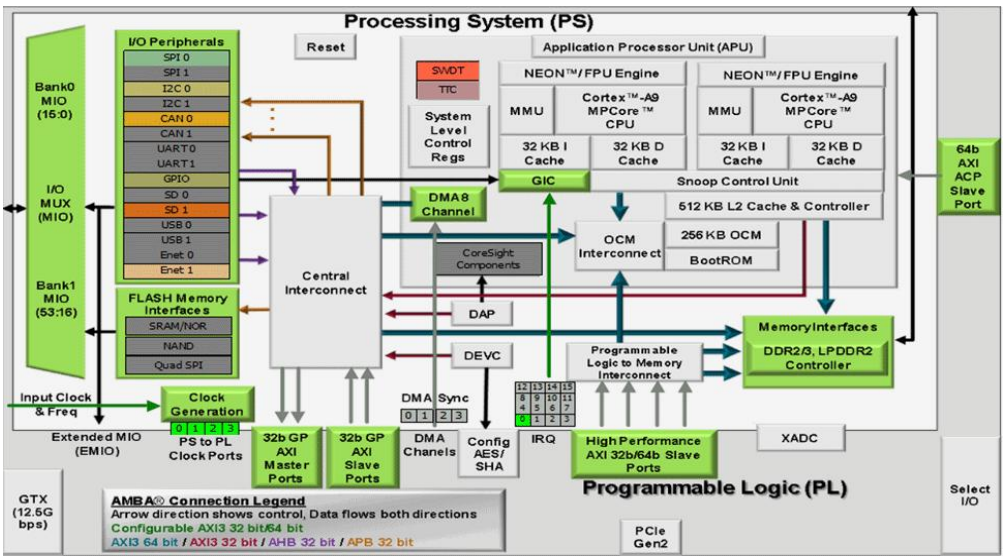

Figure 5: ZYNQ 7000 Chip General Block Diagram

The main parameters of the PL (Programmable Logic) part are as follows:

- Logic Cells: 350K
- Look-Up Tables (LUTs): 218,600
- Flip-Flops: 437,200
- 18x25 Multipliers (MACCs): 900
- Block RAM: 19.2Mb
- 16 high-speed GTX transceivers, supporting PCIe Gen2x8
- 2 ADCs (Analog to Digital Converters), capable of measuring on-chip voltage, temperature sensing, and up to 17 external differential input channels at 1MBPS

The main parameters of the PS (Processing System) part are as follows:

- Application processor based on dual-core ARM Cortex-A9, ARM-v7 architecture, up to 800MHz
- Each CPU with 32KB L1 instruction and data cache, 512KB L2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External memory interface, supporting 16/32-bit DDR2, DDR3 interfaces
- 2 Gigabit Ethernet interfaces with scatter-gather DMA, GMII, RGMII, SGMII interfaces
- 2 USB 2.0 OTG interfaces, each supporting up to 12 endpoints
- 2 CAN 2.0B bus interfaces
- 2 SD cards, SDIO, MMC compatible controllers
- 2 SPI, 2 UARTs, 2 I2C interfaces
- 54 *multi-functions* configurable IOs, which can be software-configured as general IO or peripheral control interfaces
- High-bandwidth connection within PS and from PS to PL

The XC7Z045-2FFG900I chip has a speed grade of -2, is industrial grade, and comes in an FGG900 package, with a pin pitch of 1.0mm.

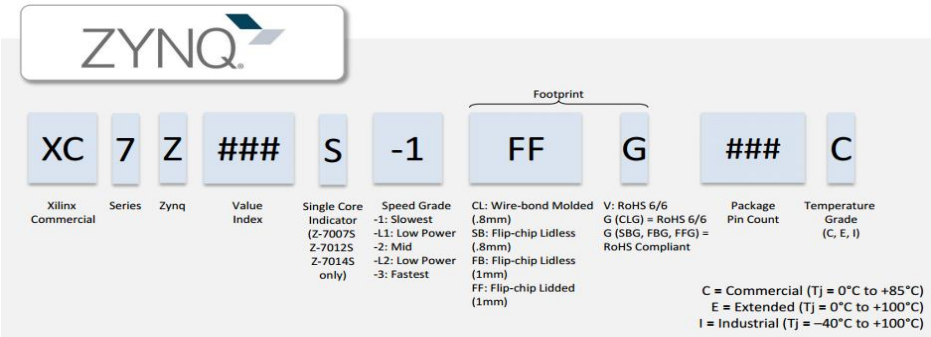

Figure 6: Definition of ZYNQ model naming rules

Figure 7: Definition of ZYNQ model naming rules

DR3 DRAM

Model and Schematic

The AC7Z045 SoM features four Micron 512MB DDR3 memory chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125), with two chips allocated to each of the PS (Processing System) and PL (Programmable Logic) sides. These two DDR3 SDRAM chips form a 32-bit bus width. The DDR3 SDRAM on the PS side can achieve a maximum operating speed of 533MHz (data rate of 1066Mbps) and is directly connected to the memory interface of the ZYNQ's Processing System (PS) at BANK 502. On the PL side, the DDR3 SDRAM can reach a maximum speed of 800MHz (data rate of 1600Mbps) and is connected to the FPGA's BANK33 and BANK34 interfaces.

The specific configuration of the DDR3 SDRAM is detailed in Table 1 below.

Position Number	Chip Type	Capacity	Manufacturers
U4, U5, U7, U8	MT41J256M16HA-125	256M x 16bit	Micron

Table 1: DDR3 SDRAM Specific Configuration

The hardware design for DDR3 requires meticulous attention to signal integrity. We have thoroughly considered aspects such as matching resistors/termination resistors, impedance control of traces, and equal length trace routing during both circuit and PCB design to ensure stable high-speed operation of DDR3.

Hardware connection schematic for the DDR3 DRAM on the PS side is shown in Figure 8:

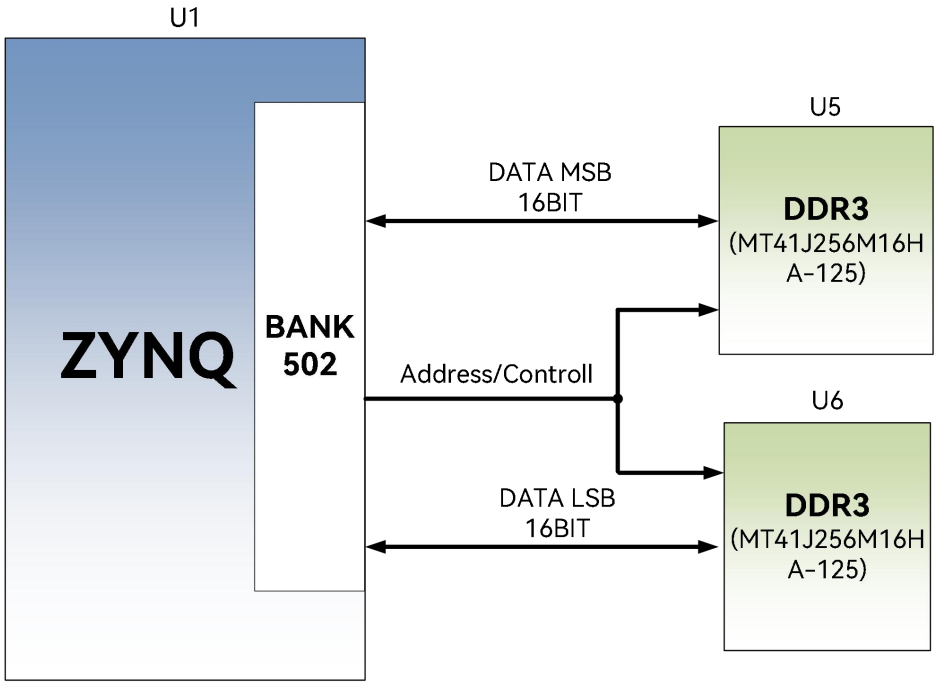

Figure 8: DDR3 DRAM Schematic Diagram (PS)

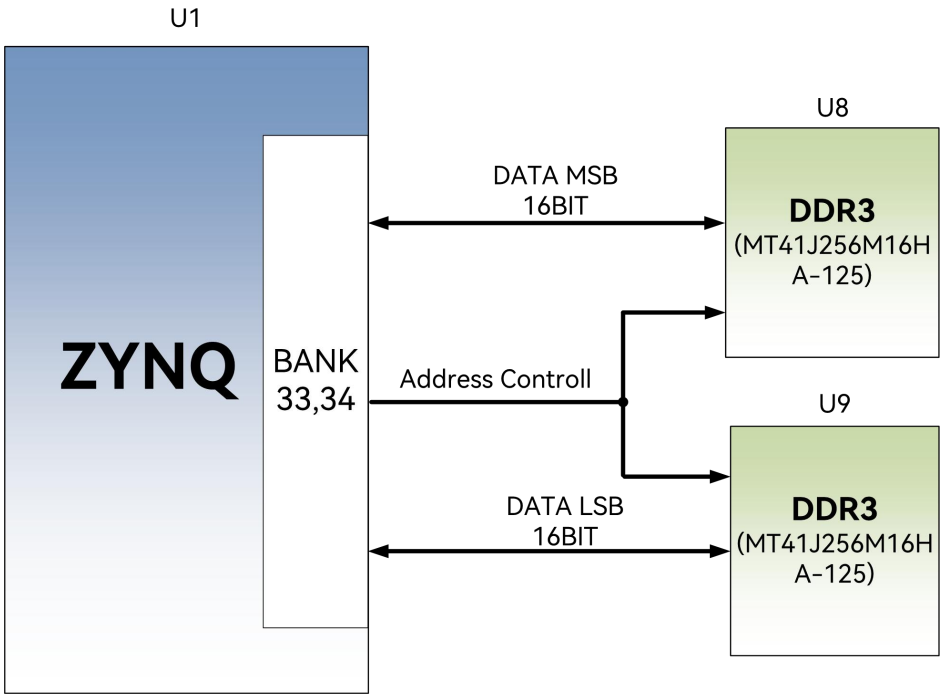

Figure 9: DDR3 DRAM Schematic Diagram (PL)

DDR3 DRAM PIN Assignment (PS):

Signal Name	ZYNQ PIN Name	ZYNQ PIN #
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	C26
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	B26
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	C29
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	B29
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	G29
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	F29
PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	L28
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	L29
PS_DDR3_D0	PS_DDR_DQ0_502	A25
PS_DDR3_D1	PS_DDR_DQ1_502	E25
PS_DDR3_D2	PS_DDR_DQ2_502	B27
PS_DDR3_D3	PS_DDR_DQ3_502	D25
PS_DDR3_D4	PS_DDR_DQ4_502	B25
PS_DDR3_D5	PS_DDR_DQ5_502	E26
PS_DDR3_D6	PS_DDR_DQ6_502	D26
PS_DDR3_D7	PS_DDR_DQ7_502	E27
PS_DDR3_D8	PS_DDR_DQ8_502	A29
PS_DDR3_D9	PS_DDR_DQ9_502	A27
PS_DDR3_D10	PS_DDR_DQ10_502	A30
PS_DDR3_D11	PS_DDR_DQ11_502	A28
PS_DDR3_D12	PS_DDR_DQ12_502	C28
PS_DDR3_D13	PS_DDR_DQ13_502	D30
PS_DDR3_D14	PS_DDR_DQ14_502	D28
PS_DDR3_D15	PS_DDR_DQ15_502	D29
PS_DDR3_D16	PS_DDR_DQ16_502	H27
PS_DDR3_D17	PS_DDR_DQ17_502	G27
PS_DDR3_D18	PS_DDR_DQ18_502	H28
PS_DDR3_D19	PS_DDR_DQ19_502	E28
PS_DDR3_D20	PS_DDR_DQ20_502	E30
PS_DDR3_D21	PS_DDR_DQ21_502	F28
PS_DDR3_D22	PS_DDR_DQ22_502	G30

PS_DDR3_D23	PS_DDR_DQ23_502	F30
PS_DDR3_D24	PS_DDR_DQ24_502	J29
Signal Name	**ZYNQ PIN Name**	**ZYNQ PIN #**
PS_DDR3_D25	PS_DDR_DQ25_502	K27
PS_DDR3_D26	PS_DDR_DQ26_502	J30
PS_DDR3_D27	PS_DDR_DQ27_502	J28
PS_DDR3_D28	PS_DDR_DQ28_502	K30
PS_DDR3_D29	PS_DDR_DQ29_502	M29
PS_DDR3_D30	PS_DDR_DQ30_502	L30
PS_DDR3_D31	PS_DDR_DQ31_502	M30
PS_DDR3_DM0	PS_DDR_DM0_502	C27
PS_DDR3_DM1	PS_DDR_DM1_502	B30
PS_DDR3_DM2	PS_DDR_DM2_502	H29
PS_DDR3_DM3	PS_DDR_DM3_502	K28
PS_DDR3_A0	PS_DDR_A0_502	L25
PS_DDR3_A1	PS_DDR_A1_502	K26
PS_DDR3_A2	PS_DDR_A2_502	L27
PS_DDR3_A3	PS_DDR_A3_502	G25
PS_DDR3_A4	PS_DDR_A4_502	J26
PS_DDR3_A5	PS_DDR_A5_502	G24
PS_DDR3_A6	PS_DDR_A6_502	H26
PS_DDR3_A7	PS_DDR_A7_502	K22
PS_DDR3_A8	PS_DDR_A8_502	F27
PS_DDR3_A9	PS_DDR_A9_502	J23
PS_DDR3_A10	PS_DDR_A10_502	G26
PS_DDR3_A11	PS_DDR_A11_502	H24
PS_DDR3_A12	PS_DDR_A12_502	K23
PS_DDR3_A13	PS_DDR_A13_502	H23
PS_DDR3_A14	PS_DDR_A14_502	J24
PS_DDR3_BA0	PS_DDR_BA0_502	M27
PS_DDR3_BA1	PS_DDR_BA1_502	M26
PS_DDR3_BA2	PS_DDR_BA2_502	M25
PS_DDR3_S0	PS_DDR_CS_B_502	N22

PS_DDR3_RAS	PS_DDR_RAS_B_502	N24
PS_DDR3_CAS	PS_DDR_CAS_B_502	M24
PS_DDR3_WE	PS_DDR_WE_B_502	N23
PS_DDR3_ODT	PS_DDR_ODT_502	L23
PS_DDR3_RESET	PS_DDR_DRST_B_502	F25
Signal Name	**ZYNQ PIN Name**	**ZYNQ PIN #**
PS_DDR3_CLK0_P	PS_DDR_CKP_502	K25
PS_DDR3_CLK0_N	PS_DDR_CKN_502	J25
PS_DDR3_CKE	PS_DDR_CKE_502	M22

Table 2: DDR3 DRAM PIN Assignment (PS)

DR3 DRAM PIN Assignment (PL):

Signal Name	ZYNQ PIN Name	ZYNQ PIN #
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_33	K3
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_33	K2
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_33	J1
PL_DDR3_DQS1_N	IO_L9N_T1_DQS_33	H1
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_33	E6
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_33	D5
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_33	A5
PL_DDR3_DQS4_N	IO_L21N_T3_DQS_33	A4
PL_DDR3_D0	IO_L1N_T0_33	J3
PL_DDR3_D1	IO_L4N_T0_33	L2
PL_DDR3_D2	IO_L1P_T0_33	J4
PL_DDR3_D3	IO_L4P_T0_33	L3
PL_DDR3_D4	IO_L2N_T0_33	K1
PL_DDR3_D5	IO_L6P_T0_33	K6
PL_DDR3_D6	IO_L5N_T0_33	J5
PL_DDR3_D7	IO_L5P_T0_33	K5
PL_DDR3_D8	IO_L11P_T1_SRCC_33	H4
PL_DDR3_D9	IO_L10N_T1_33	G1
PL_DDR3_D10	IO_L8P_T1_33	H6
PL_DDR3_D11	IO_L7N_T1_33	F2

PL_DDR3_D12	IO_L10P_T1_33	H2
PL_DDR3_D13	IO_L12N_T1_MRCC_33	G4
PL_DDR3_D14	IO_L8N_T1_33	G6
PL_DDR3_D15	IO_L11N_T1_SRCC_33	H3
PL_DDR3_D16	IO_L18P_T2_33	E1
PL_DDR3_D17	IO_L17P_T2_33	E3
PL_DDR3_D18	IO_L16N_T2_33	D3
PL_DDR3_D19	IO_L14P_T2_SRCC_33	F4
PL_DDR3_D20	IO_L18N_T2_33	D1
PL_DDR3_D21	IO_L13N_T2_MRCC_33	E5
PL_DDR3_D22	IO_L16P_T2_33	D4
PL_DDR3_D23	IO_L17N_T2_33	E2
PL_DDR3_D24	IO_L22P_T3_33	C2
PL_DDR3_D25	IO_L24N_T3_33	A2
PL_DDR3_D26	IO_L20N_T3_33	B4
Signal Name	**ZYNQ PIN Name**	**ZYNQ PIN #**
PL_DDR3_D27	IO_L20P_T3_33	B5
PL_DDR3_D28	IO_L22N_T3_33	C1
PL_DDR3_D29	IO_L24P_T3_33	A3
PL_DDR3_D30	IO_L19P_T3_33	C4
PL_DDR3_D31	IO_L23P_T3_33	B2
PL_DDR3_DM0	IO_L2P_T0_33	L1
PL_DDR3_DM1	IO_L12P_T1_MRCC_33	G5
PL_DDR3_DM2	IO_L14N_T2_SRCC_33	F3
PL_DDR3_DM3	IO_L23N_T3_33	B1
PL_DDR3_A0	IO_L18P_T2_34	H7
PL_DDR3_A1	IO_L21P_T3_DQS_34	L8
PL_DDR3_A2	IO_L7N_T1_34	H11
PL_DDR3_A3	IO_L10N_T1_34	D10
PL_DDR3_A4	IO_L15N_T2_DQS_34	H8
PL_DDR3_A5	IO_L8N_T1_34	D11
PL_DDR3_A6	IO_L19P_T3_34	L7
PL_DDR3_A7	IO_L10P_T1_34	E10

PL_DDR3_A8	IO_L23P_T3_34	L10
PL_DDR3_A9	IO_L9P_T1_DQS_34	H12
PL_DDR3_A10	IO_L18N_T2_34	G7
PL_DDR3_A11	IO_L20N_T3_34	J9
PL_DDR3_A12	IO_L13P_T2_MRCC_34	H9
PL_DDR3_A13	IO_L7P_T1_34	J11
PL_DDR3_A14	IO_L22N_T3_34	K10
PL_DDR3_BA0	IO_L22P_T3_34	K11
PL_DDR3_BA1	IO_L21N_T3_DQS_34	K8
PL_DDR3_BA2	IO_L9N_T1_DQS_34	G11
PL_DDR3_S0	IO_L16P_T2_34	F8
PL_DDR3_RAS	IO_L13N_T2_MRCC_34	G9
PL_DDR3_CAS	IO_L17P_T2_34	E7
PL_DDR3_WE	IO_L16N_T2_34	F7
PL_DDR3_ODT	IO_L20P_T3_34	J10
PL_DDR3_RESET	IO_L8P_T1_34	E11
PL_DDR3_CLK0_P	IO_L12P_T1_MRCC_34	D9
PL_DDR3_CLK0_N	IO_L12N_T1_MRCC_34	D8
PL_DDR3_CKE	IO_L17N_T2_34	D6

Table 3: DDR3 DRAM PIN Assignment (PL)

1.2 QSPI Flash

Model and Schematic

The SoM is equipped with two 256Mbit Quad-SPI FLASH chips forming an 8-bit wide data bus, with the model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can serve as the boot device for the system to store boot images. These images include the FPGA's bit file, application code for the ARM processors, and other user data files.

The specific model and related parameters of the QSPI FLASH are listed in Table 4.

Position Number	Chip Type	Capacity	Manufacturers
U13, U14	W25Q256FVEI	256M bit	Winbond

Table 4: QSPI Flash Model and Specifications

The QSPI FLASH is connected to the GPIO pins of the ZYNQ chip's PS section at BANK500. In system design, these GPIO pins on the PS side need to be configured to function as the QSPI FLASH interface.

Figure 10 shows the section of the QSPI Flash in the schematic diagram.

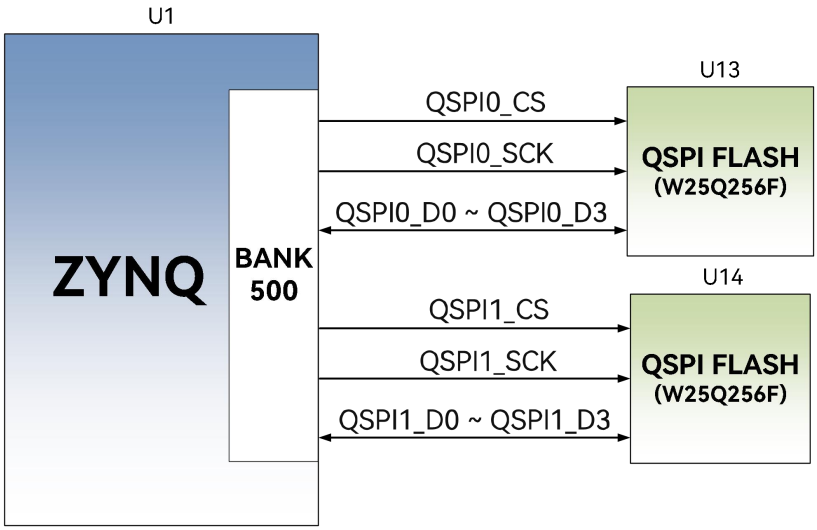

Figure 10: QSPI Flash Schematic Diagram

QSPI Flash PIN Assignment:

Signal Name	ZYNQ PIN Name	ZYNQ PIN #
QSPI0_SCK	PS_MIO6_500	D24
QSPI0_CS	PS_MIO1_500	D23
QSPI0_D0	PS_MIO2_500	F23
QSPI0_D1	PS_MIO3_500	C23
QSPI0_D2	PS_MIO4_500	E23
QSPI0_D3	PS_MIO5_500	C24
QSPI1_SCK	PS_MIO9_500	A24
QSPI1_CS	PS_MIO0_500	F24
QSPI1_D0	PS_MIO10_500	E22
QSPI1_D1	PS_MIO11_500	A23
QSPI1_D2	PS_MIO12_500	E21
QSPI1_D3	PS_MIO13_500	F22

Table 5: QSPI Flash PIN Assignment

1.3 eMMC Flash

Model and Schematic

The SoM includes one high-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with voltage levels of either 1.8V or 3.3V. The data bus width between the eMMC FLASH and the ZYNQ is 4 bits. Due to its large capacity and non-volatile nature, the eMMC FLASH can serve as a significant storage device within the ZYNQ system, storing ARM applications, system files, and other user data files.

Position Number	Chip Type	Capacity	Manufacturers
U15	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 6: eMMC FLASH Model and Parameters

The eMMC FLASH is connected to the GPIO pins of the ZYNQ chip's PS section at BANK501. In system design, these GPIO pins on the PS side need to be configured to function as an SD interface.

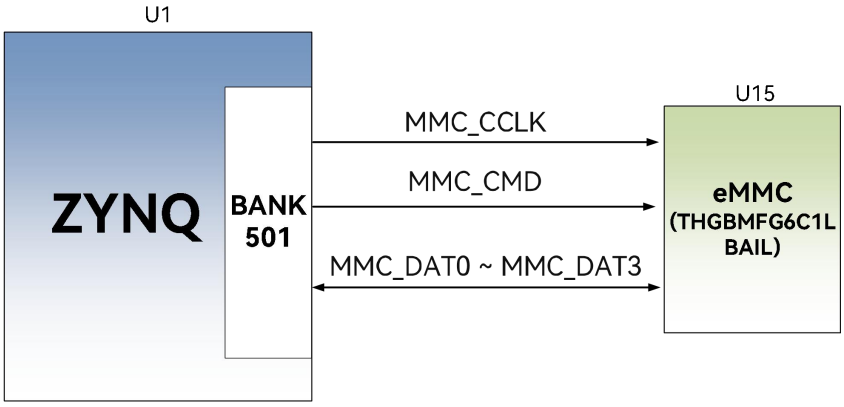

Figure 11: eMMC Flash Schematic Diagram

eMMC Flash PIN Assignment

Signal Name	ZYNQ PIN Name	ZYNQ PIN #
MMC_CCLK	PS_MIO48_501	C19
MMC_CMD	PS_MIO47_501	A18
MMC_D0	PS_MIO46_501	F20
MMC_D1	PS_MIO49_501	D18
MMC_D2	PS_MIO50_501	A19
MMC_D3	PS_MIO51_501	F19

Table 7: eMMC Flash PIN Assignment

1.4 Clock configuration

Model and Schematic

The SoM provides reference clocks for the PS system, the PL logic section, and the GTX transceivers, allowing the PS and PL to operate independently.

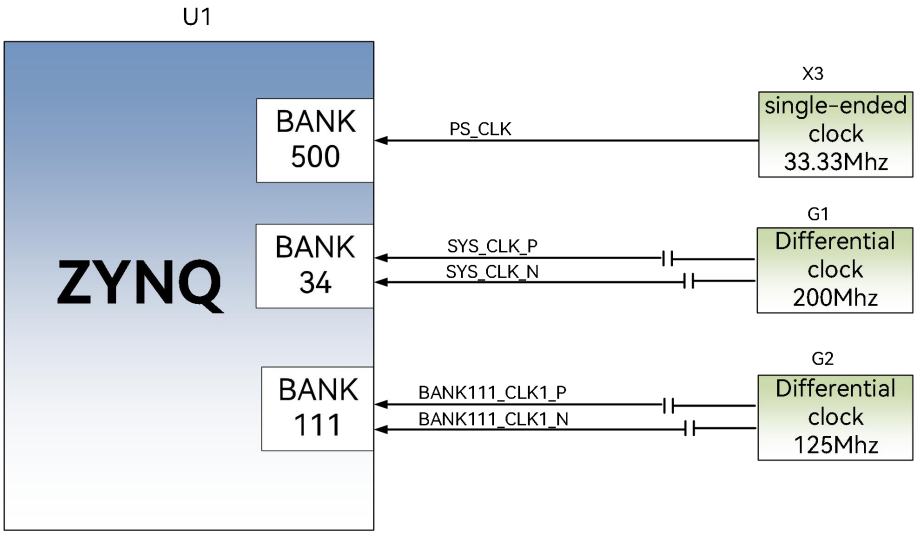

Figure 11: eMMC Flash Schematic Diagram

PS System Clock Source

The ZYNQ chip receives a 33.333MHz clock input for the PS section from the X4 crystal oscillator on the SoM. This clock input is connected to the PS_CLK_500 pin on BANK500 of the ZYNQ chip.

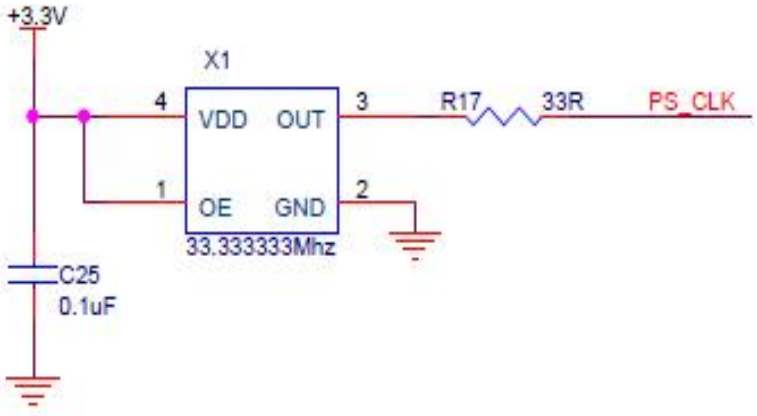

Figure 12: Active Crystal Oscillator for the PS Section

Clock PIN Assignment (PS)

Signal Name	ZYNQ PIN #
PS_CLK	A22

Table 8: Clock PIN Assignment (PS)

PL System Clock Source

The board provides a differential 200MHz clock source for the PL system, serving as the reference clock for the DDR3 controller. The oscillator output is connected to the global clock (MRCC) of FPGA BANK34, which can be used to drive both the DDR3 controller and user logic within the FPGA.

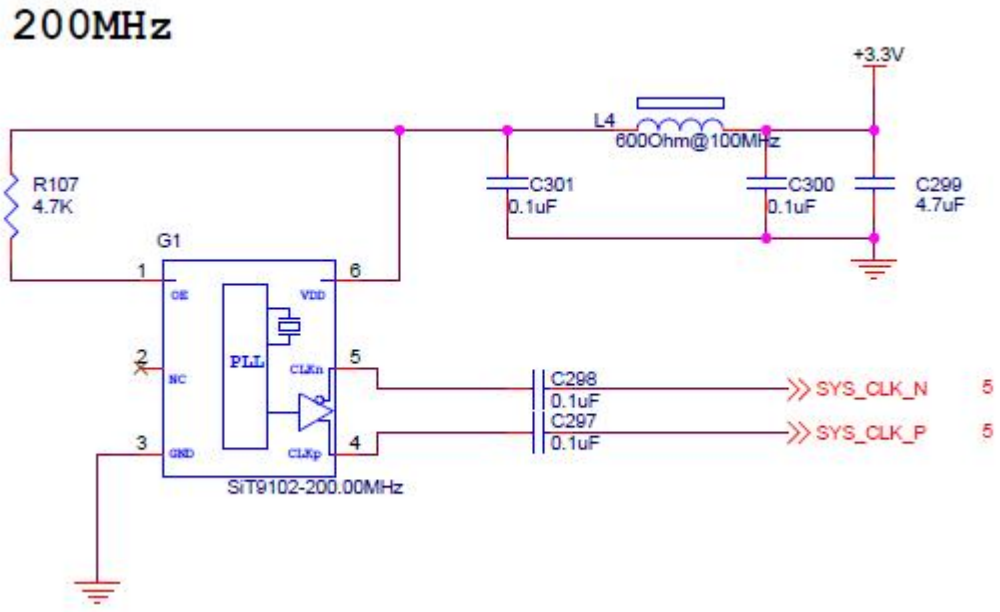

Figure 13: PL System Clock Source

Clock PIN assignment (PL)

Signal Name	ZYNQ PIN #
SYS_CLK_P	F9
SYS_CLK_N	E8

Table 9: Clock PIN Assignment (PL)

GTX Reference Clock

The SoM provides a 125MHz reference clock for the GTX transceivers. The reference clock is connected to the REFCLK1P/REFCLK1N inputs on BANK110.

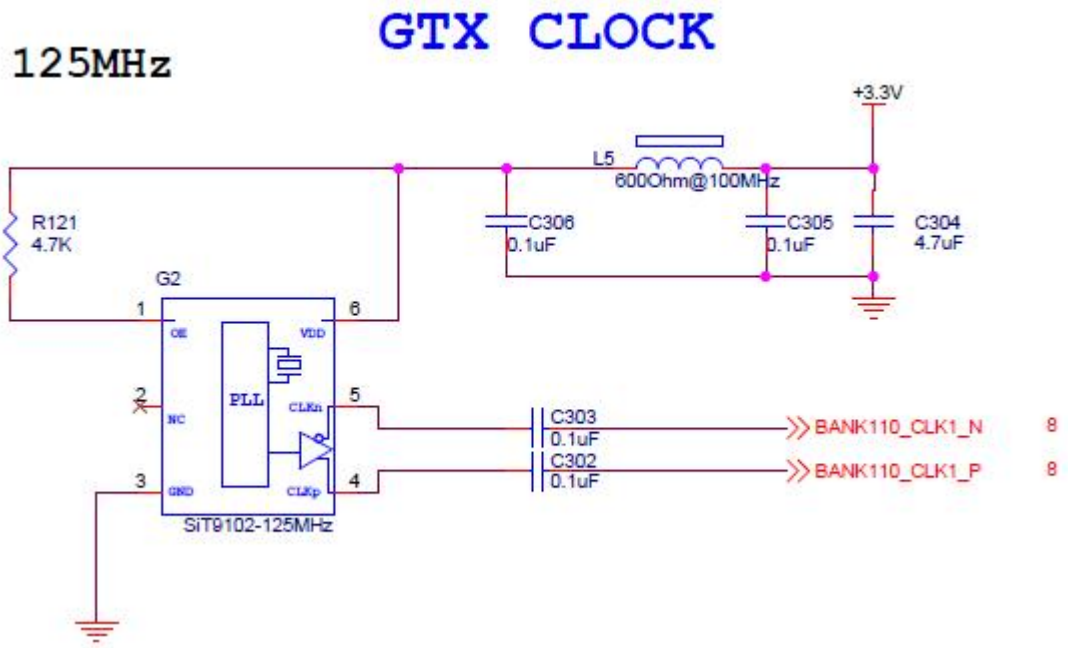

Figure 14: GTX Clock Source

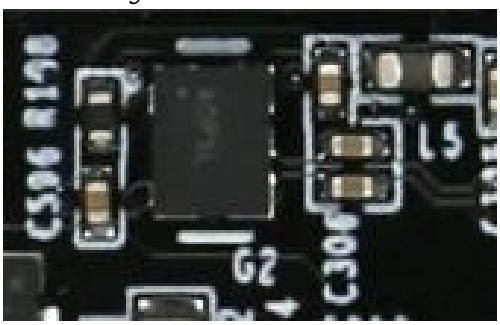

Figure 15: GTX Clock Source Real Product

GTX Clock Source PIN Assignment

Signal Name	ZYNQ PIN #
BANK110_CLK1_P	AC8
BANK110_CLK1_N	AC7

Table 10: GTX Clock Source PIN Assignment

1.5 LED

The AC7Z045 SoM features two red LEDs, one for power indication (PWR) and one for configuration status (DONE). The power LED will light up when power is applied; after the FPGA configuration program is loaded, the configuration LED will illuminate.

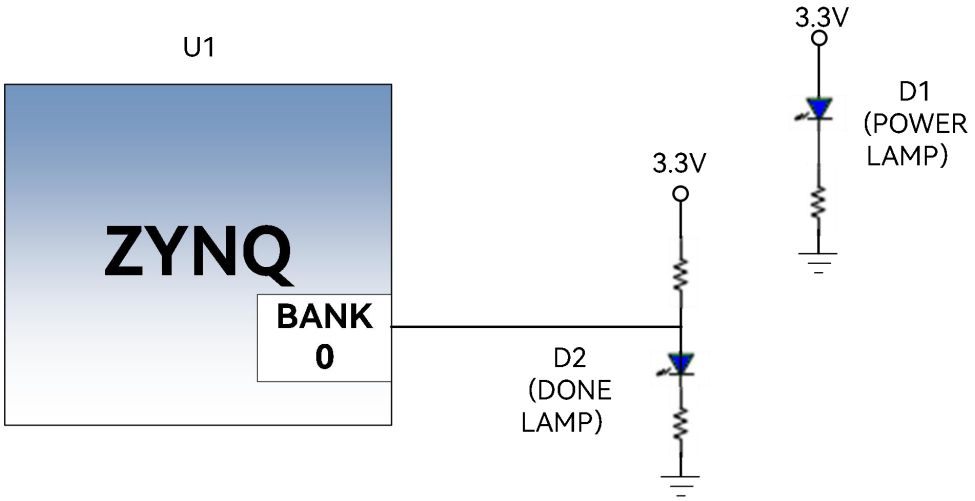

Figure 16: LED Schematic Diagram

1.6 Reset Circuit

The AC7Z045 SoM includes a reset circuit. The reset input signal is connected to a reset button on the baseboard, and the reset output is connected to the PS reset pin of the ZYNQ chip. Users can utilize this baseboard button to reset the ZYNQ system.

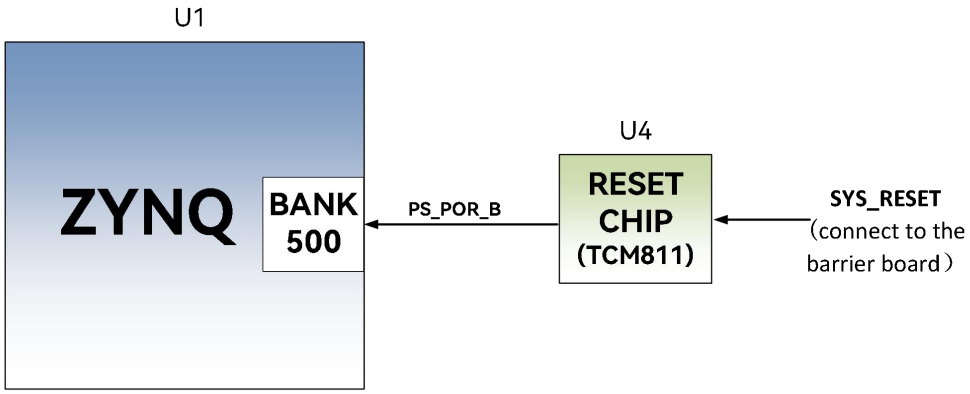

Figure 17: Reset Circuit Schematic Diagram

Signal Name	ZYNQ PIN Name	ZYNQ PIN #	Comments
PS_POR_B	PS_POR_B_500	D21	ZYNQ System Reset Signal

Table 11: Reset Button PIN Assignment

1.7 Power Supply

Model and Schematic

The AC7Z045 SoM operates with a supply voltage of DC 5V, which is provided through a connection to the baseboard. The schematic diagram of the power supply design on the board is shown in Figure 18:

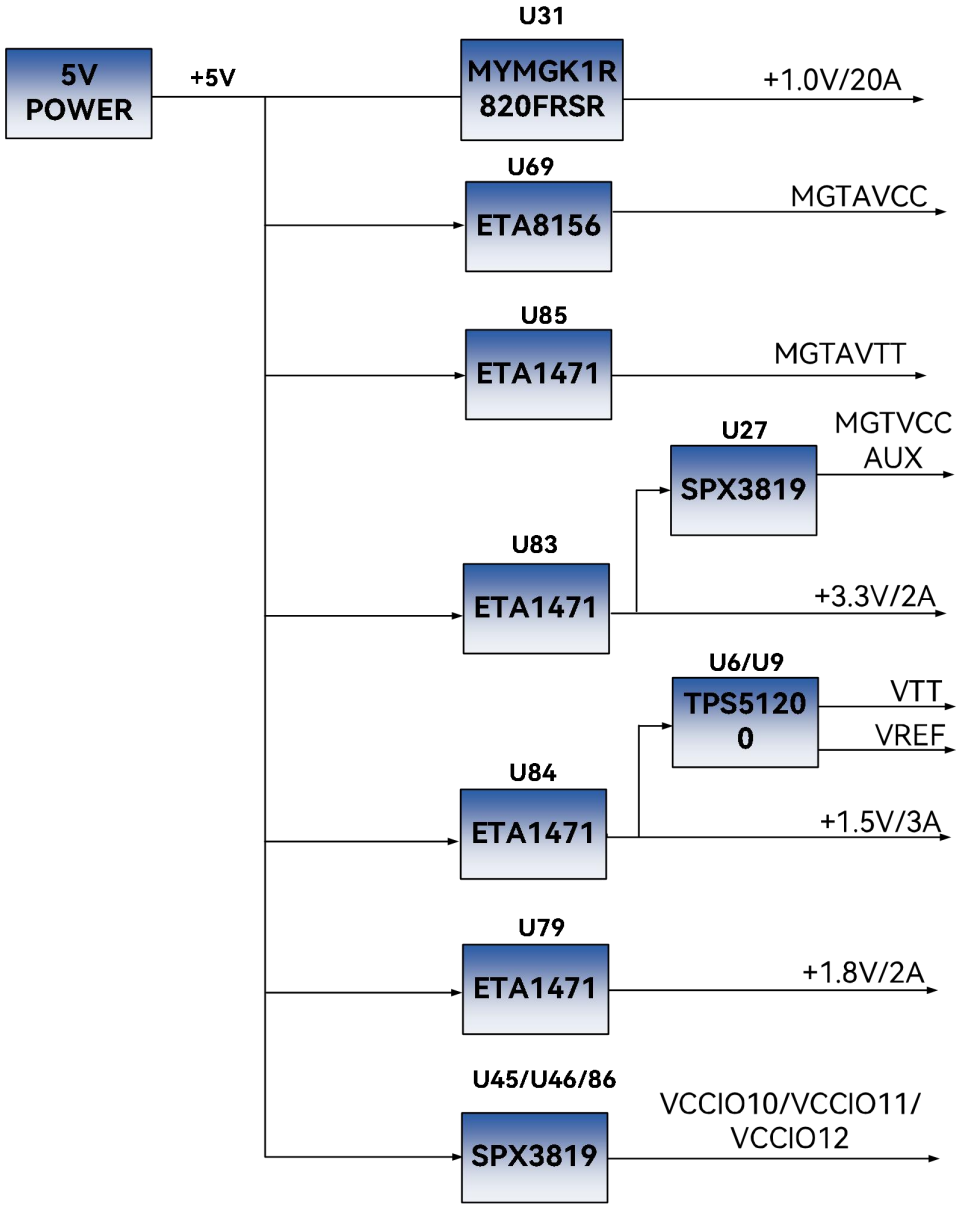

Figure 18: Power Supply Interface Schematic Diagram

The +5V supply is converted by the DCDC power chip MYMGK1R820FRSR to produce the +1.0V core voltage for the ZYNQ, with the +1.0V power output capable of reaching up to 20A, which significantly exceeds the current requirements for the ZYNQ's core voltage. The +5V power is further processed by the DCDC chip ETA1471 to generate four voltage rails: MGTAVTT, +1.5V, +3.3V, and another +1.5V.

The MGTAVTT supply is generated using the DCDC chip ETA8156, and +3.3V is converted by an LDO chip SPX3819-1-8 to produce the +1.8V auxiliary power for the GTX. The VTT and VREF voltages for the DDR3 memory on both the PS and PL sections are generated by the TPS51200. Additionally, three SPX3819M5-3-3 chips produce the IO supply for BANK10, BANK11, and BANK12, allowing users to change the LDO chips to adjust these BANKs' IO inputs/outputs to different voltage standards.

Power Supply	Function
+1.0V	ZYNQ PS and PL partial core voltage
+1.8V	ZYNQ PS and PL partial Auxiliary Voltage, BANK501, BANK3, eMMC
+3.3V	ZYNQ Bank0, Bank500, QSIP FLASH, Clock Crystal Oscillator
+1.5V	DDR3, ZYNQ Bank502, Bank33, Bank34
VCCIO10	ZYNQ Bank10
VCCIO11	ZYNQ Bank11
VCCIO12	ZYNQ Bank12
VREF, VTT（+0.75V）	PS DDR3，PL DDR3
MGTAVCC(+1.0V)	ZYNQ Bank111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank111, Bank112
MGTVCCAUX（+1.8V）	ZYNQ Bank111, Bank112

Table 12: Power Supply Interface Function

Due to the power-up sequence requirements of the ZYNQ FPGA, in our circuit design, the product has followed the chip's power specifications. The power-up sequence is designed as follows: +1.0V -> +1.8V -> (+1.5V, +3.3V, VCCIO), ensuring the proper operation of the chip.

1.8 Structure

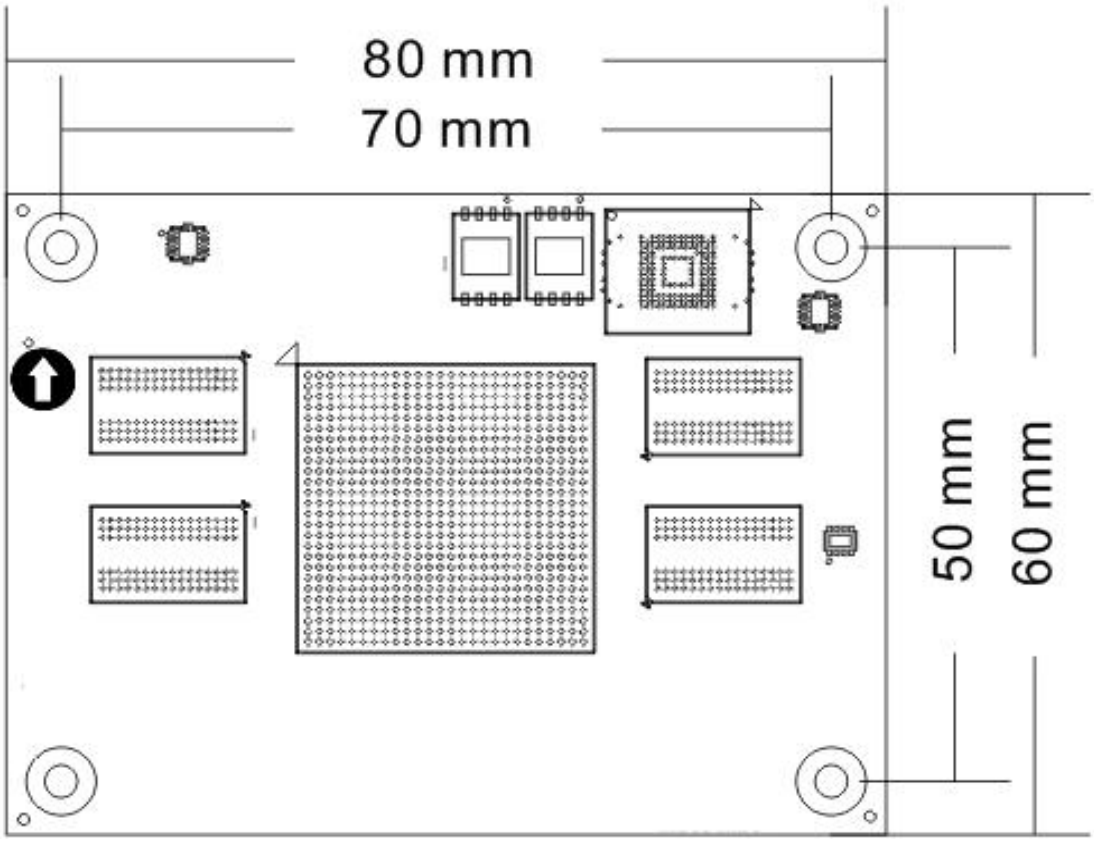

Figure 19: SoM Structure Top View

1.9 Connector PIN Assignment

The SoM extends four high-speed expansion ports, interfacing with the base board through four 120-pin board-to-board connectors (J29 to J32). The connectors used are Panasonic's AXK5A2137YG, with the corresponding connectors on the base board being model AXK6A2337YG.

The tables are shown on the next page.

J29 Connector PIN Assignment:

J29 PIN	Signal Name	ZYNQ PIN	J29 PIN	Signal Name	ZYNQ PIN
1	B11_L4_N	AJ24	2	B11_L1_N	AK25
3	B11_L4_P	AJ23	4	B11_L1_P	AJ25
5	GND	-	6	GND	-
7	B11_L3_P	AJ21	8	B11_L8_N	AG25
9	B11_L3_N	AK21	10	B11_L8_P	AG24
11	GND	-	12	GND	-
13	B11_L2_N	AK23	14	B11_L12_N	AF22
15	B11_L2_P	AK22	16	B11_L12_P	AE22
17	GND	-	18	GND	-
19	B11_L5_N	AH24	20	B11_L16_N	AK18
21	B11_L5_P	AH23	22	B11_L16_P	AK17
23	GND	-	24	GND	-
25	B11_L15_P	AJ20	26	B11_L6_N	AH22
27	B11_L15_N	AK20	28	B11_L6_P	AG22
29	GND	-	30	GND	-
31	B11_L13_N	AH21	32	B11_L17_N	AJ19
33	B11_L13_P	AG21	34	B11_L17_P	AH19
35	GND	-	36	GND	-
37	B11_L14_N	AG20	38	B11_L18_N	AG19
39	B11_L14_P	AF20	40	B11_L18_P	AF19
41	GND	-	42	GND	-
43	B11_L19_P	AB21	44	B11_L20_N	Y21
45	B11_L19_N	AB22	46	B11_L20_P	W21
47	GND	-	48	GND	-
49	B10_L13_P	AG17	50	B10_L17_P	AE18
51	B10_L13_N	AG16	52	B10_L17_N	AE17
53	GND	-	54	GND	-
55	B10_L2_P	AH18	56	B10_L15_P	AF18
57	B10_L2_N	AJ18	58	B10_L15_N	AF17
59	GND	-	60	GND	-
61	B10_L4_P	AJ16	62	B10_L6_P	AH17

63	B10_L4_N	AK16	64	B10_L6_N	AH16
65	GND	-	66	GND	-
J29 PIN	**Signal Name**	**ZYNQ PIN #**	**J29 PIN**	**Signal Name**	**ZYNQ PIN #**
67	B10_L16_P	AE16	68	B10_L24_N	AB16
69	B10_L16_N	AE15	70	B10_L24_P	AB17
71	GND	-	72	GND	-
73	B10_L20_P	AA15	74	B10_L5_N	AK15
75	B10_L20_N	AA14	76	B10_L5_P	AJ15
77	GND	-	78	GND	-
79	B10_L18_P	AD16	80	B10_L23_P	AC17
81	B10_L18_N	AD15	82	B10_L23_N	AC16
83	GND	-	84	GND	-
85	B10_L14_N	AG15	86	B10_L12_P	AF14
87	B10_L14_P	AF15	88	B10_L12_N	AG14
89	GND	-	90	GND	-
91	B10_L1_P	AK13	92	B10_L22_P	AB15
93	B10_L1_N	AK12	94	B10_L22_N	AB14
95	GND	-	96	GND	-
97	B10_L8_P	AH14	98	B10_L3_P	AJ14
99	B10_L8_N	AH13	100	B10_L3_N	AJ13
101	GND	-	102	GND	-
103	B10_L10_N	AH12	104	B10_L11_N	AF13
105	B10_L10_P	AG12	106	B10_L11_P	AE13
107	GND	-	108	GND	-
109	B10_L7_N	AF12	110	B10_L9_P	AD14
111	B10_L7_P	AE12	112	B10_L9_N	AD13
113	GND	-	114	GND	-
115	B10_L19_P	AC14	116	B10_L21_N	AC12
117	B10_L19_N	AC13	118	B10_L21_P	AB12
119	GND	-	120	GND	-

Table 13: J29 Connector PIN Assignment

J30 Connector PIN Assignment

J30 PIN	Signal Name	ZYNQ PIN	J30 PIN	Signal Name	ZYNQ PIN
1	BANK111_TX0_N	AB1	2	BANK111_RX0_N	AC3
3	BANK111_TX0_P	AB2	4	BANK111_RX0_P	AC4
5	GND	-	6	GND	-
7	BANK111_TX1_N	Y1	8	BANK111_RX1_N	AB5
9	BANK111_TX1_P	Y2	10	BANK111_RX1_P	AB6
11	GND	-	12	GND	-
13	BANK111_TX2_N	W3	14	BANK111_RX2_N	Y5
15	BANK111_TX2_P	W4	16	BANK111_RX2_P	Y6
17	GND	-	18	GND	-
19	BANK111_TX3_N	V1	20	BANK111_RX3_N	AA3
21	BANK111_TX3_P	V2	22	BANK111_RX3_P	AA4
23	GND	-	24	GND	-
25	BANK111_CLK0_N	U7	26	BANK111_CLK1_N	W7
27	BANK111_CLK0_P	U8	28	BANK111_CLK1_P	W8
29	GND	-	30	GND	-
31	BANK112_TX0_N	T1	32	BANK112_RX0_N	V5
33	BANK112_TX0_P	T2	34	BANK112_RX0_P	V6
35	GND	-	36	GND	-
37	BANK112_TX1_N	R3	38	BANK112_RX1_N	U3
39	BANK112_TX1_P	R4	40	BANK112_RX1_P	U4
41	GND	-	42	GND	-
43	BANK112_TX2_N	P1	44	BANK112_RX2_N	T5
45	BANK112_TX2_P	P2	46	BANK112_RX2_P	T6
47	GND	-	48	GND	-
49	BANK112_TX3_N	N3	50	BANK112_RX3_N	P5
51	BANK112_TX3_P	N4	52	BANK112_RX3_P	P6
53	GND	-	54	GND	-
55	BANK112_CLK0_N	N7	56	BANK112_CLK1_N	R7
57	BANK112_CLK0_P	N8	58	BANK112_CLK1_P	R8
59	GND	-	60	GND	-
61	BANK109_RX2_N	AG7	62	BANK110_RX0_N	AH5

63	BANK109_RX2_P	AG8	64	BANK110_RX0_P	AH6
65	GND	-	66	GND	-
J30 PIN	**Signal Name**	**ZYNQ PIN**	**J30 PIN**	**Signal Name**	**ZYNQ PIN**
67	BANK109_RX3_N	AE7	68	BANK110_TX0_N	AH1
69	BANK109_RX3_P	AE8	70	BANK110_TX0_P	AH2
71	GND	-	72	GND	-
73	BANK109_RX1_P	AJ8	74	BANK110_RX1_N	AG3
75	BANK109_RX1_N	AJ7	76	BANK110_RX1_P	AG4
77	GND	-	78	GND	-
79	BANK109_TX1_P	AK6	80	BANK110_TX1_N	AF1
81	BANK109_TX1_N	AK5	82	BANK110_TX1_P	AF2
83	GND	-	84	GND	-
85	BANK109_TX2_P	AJ4	86	BANK110_RX2_N	AF5
87	BANK109_TX2_N	AJ3	88	BANK110_RX2_P	AF6
89	GND	-	90	GND	-
91	BANK109_TX3_P	AK2	92	BANK110_TX2_N	AE3
93	BANK109_TX3_N	AK1	94	BANK110_TX2_P	AE4
95	GND	AA12	96	GND	-
97	BANK109_TX0_N	AK9	98	BANK110_RX3_N	AD5
99	BANK109_TX0_P	AK10	100	BANK110_RX3_P	AD6
101	GND	-	102	GND	-
103	BANK109_RX0_N	AH9	104	BANK110_TX3_N	AD1
105	BANK109_RX0_P	AH10	106	BANK110_TX3_P	AD2
107	GND	-	108	GND	-
109	BANK109_CLK0_N	AD9	110	BANK110_CLK0_N	AA7
111	BANK109_CLK0_P	AD10	112	BANK110_CLK0_P	AA8
113	GND	-	114	GND	-
115			116		
117			118		
119	GND	AA12	120	GND	AA12

Table 14: J30 Connector PIN Assignment

J31 Connector PIN Assignment

J31 PIN	Signal Name	ZYNQ PIN	J31 PIN	Signal Name	ZYNQ PIN
1	FPGA_TCK	Y12	2	FPGA_TDI	P10
3	FPGA_TMS	V10	4	FPGA_TDO	Y10
5	GND	-	6	GND	-
7	B35_L2_P	J13	8	B35_L8_N	G14
9	B35_L2_N	H13	10	B35_L8_P	G15
11	GND	-	12	GND	-
13	B35_L9_P	G12	14	B35_L3_N	K13
15	B35_L9_N	F12	16	B35_L3_P	L13
17	GND	-	18	GND	-
19	B35_L22_N	B11	20	B35_L5_P	K15
21	B35_L22_P	C11	22	B35_L5_N	J15
23	GND	-	24	GND	-
25	B35_L20_N	B12	26	B35_L10_P	F13
27	B35_L20_P	C12	28	B35_L10_N	E12
29	GND	-	30	GND	AA12
31	B35_L19_N	C13	32	B35_L12_N	F14
33	B35_L19_P	C14	34	B35_L12_P	F15
35	GND	-	36	GND	-
37	B35_L24_N	A12	38	B35_L11_N	D13
39	B35_L24_P	A13	40	B35_L11_P	E13
41	GND	-	42	GND	-
43	B35_L4_N	H14	44	B35_L23_P	B14
45	B35_L4_P	J14	46	B35_L23_N	A14
47	GND	-	48	GND	-
49	B35_L1_N	L14	50	B35_L21_P	B15
51	B35_L1_P	L15	52	B35_L21_N	A15
53	GND	-	54	GND	-
55	B35_L16_N	C16	56	B35_L14_P	D15
57	B35_L16_P	D16	58	B35_L14_N	D14
59	GND	-	60	GND	-
61	B35_L18_N	A17	62	B35_L13_N	E15

63	B35_L18_P	B17	64	B35_L13_P	E16
65	GND	-	66	GND	-
J31 PIN	**Signal Name**	**ZYNQ PIN**	**J31 PIN**	**Signal Name**	**ZYNQ PIN**
67	B35_L15_N	E17	68	B35_L17_N	B16
69	B35_L15_P	F17	70	B35_L17_P	C17
71	GND	-	72	GND	-
73	B35_L7_N	G16	74	B12_L17_N	AG27
75	B35_L7_P	G17	76	B12_L17_P	AG26
77	GND	-	78	GND	-
79	B35_L6_N	H16	80	B12_L18_N	AF25
81	B35_L6_P	J16	82	B12_L18_P	AE25
83	GND	-	84	GND	-
85	B12_L6_N	AB26	86	B12_L10_N	AE26
87	B12_L6_P	AB25	88	B12_L10_P	AD25
89	GND	-	90	GND	-
91	B12_L11_N	AC27	92	B12_L13_N	AF28
93	B12_L11_P	AB27	94	B12_L13_P	AE28
95	GND	-	96	GND	-
97	B12_L12_N	AD28	98	B12_L16_N	AG30
99	B12_L12_P	AC28	100	B12_L16_P	AF30
101	GND	-	102	GND	-
103	B12_L9_N	AD29	104	B12_L22_N	AK28
105	B12_L9_P	AC29	106	B12_L22_P	AK27
107	GND	-	108	GND	-
109	B12_L14_N	AF27	110	B12_L20_N	AK30
111	B12_L14_P	AE27	112	B12_L20_P	AJ30
113	GND	-	114	GND	-
115	PS_POR_B		116	B12_L23_N	AH27
117	SYS_RESET	-	118	B12_L23_P	AH26
119	GND	-	120	GND	-

Table 15: J31 Connector PIN Assignment

J32 Connector PIN Assignment

J32 PIN	Signal Name	ZYNQ PIN	J32 PIN	Signal Name	ZYNQ PIN
1	PS_MIO5	C24	2	PS_MIO17	K21
3	PS_MIO4	E23	4	PS_MIO18	K20
5	GND	-	6	GND	-
7	PS_MIO14	B22	8	PS_MIO19	J20
9	PS_MIO15	C22	10	PS_MIO20	M20
11	GND	-	12	GND	-
13	PS_MIO52	D19	14	PS_MIO16	L19
15	PS_MIO53	C18	16	PS_MIO21	J19
17	GND	-	18	GND	-
19	PS_MIO7	B24	20	PS_MIO26	M17
21			22	PS_MIO25	G19
23	GND	-	24	GND	-
25	PS_MIO40	B20	26	PS_MIO24	M19
27	PS_MIO41	J18	28	PS_MIO23	J21
29	GND	-	30	GND	-
31	PS_MIO42	D20	32	PS_MIO27	G20
33	PS_MIO43	E18	34	PS_MIO22	L20
35	GND	-	36	GND	-
37	PS_MIO44	E20	38	PS_MIO30	L18
39	PS_MIO45	H18	40	PS_MIO29	H22
41	GND	-	42	GND	-
43	B12_L2_N	AB30	44	PS_MIO36	H17
45	B12_L2_P	AB29	46	PS_MIO31	H21
47	GND	-	48	GND	-
49	B12_L4_N	AA29	50	PS_MIO32	K17
51	B12_L4_P	Y28	52	PS_MIO33	G22
53	GND	-	54	GND	-
55	B12_L19_P	AH28	56	PS_MIO34	K18
57	B12_L19_N	AH29	58	PS_MIO35	G21
59	GND	-	60	GND	-
61	B12_L3_P	Y26	62	PS_MIO28	L17

63	B12_L3_N	Y27	64	PS_MIO37	B21
65	GND	-	66	GND	-
67	B12_L5_P	AA27	68	PS_MIO38	A20
69	B12_L5_N	AA28	70	PS_MIO39	F18
71	GND	-	72	GND	-
73	B12_L8_N	AE30	74	B12_L21_P	AJ28
75	B12_L8_P	AD30	76	B12_L21_N	AJ29
77	GND	-	78	GND	-
79	B12_L15_N	AG29	80	B12_L7_N	AD26
81	B12_L15_P	AF29	82	B12_L7_P	AC26
83	GND	-	84	GND	-
85	B11_L23_N	AA23	86	B11_L11_P	AD23
87	B11_L23_P	AA22	88	B11_L11_N	AE23
89	GND	-	90	GND	-
91	B11_L21_N	Y23	92	B11_L9_P	AF23
93	B11_L21_P	Y22	94	B11_L9_N	AF24
95	GND	-	96	GND	-
97	B11_L22_N	AB24	98	B11_L10_N	AE21
99	B11_L22_P	AA24	100	B11_L10_P	AD21
101	GND	-	102	GND	-
103	B11_L7_P	AC24	104	B11_L24_P	AC22
105	B11_L7_N	AD24	106	B11_L24_N	AC23
107	+5V	-	108	+5V	-
109	+5V	-	110	+5V	-
111	+5V	-	112	+5V	-
113	+5V	-	114	+5V	-
115	+5V	-	116	+5V	-
117	+5V	-	118	+5V	-
119	+5V	-	120	+5V	-

Table 16: J32 Connector PIN Assignment